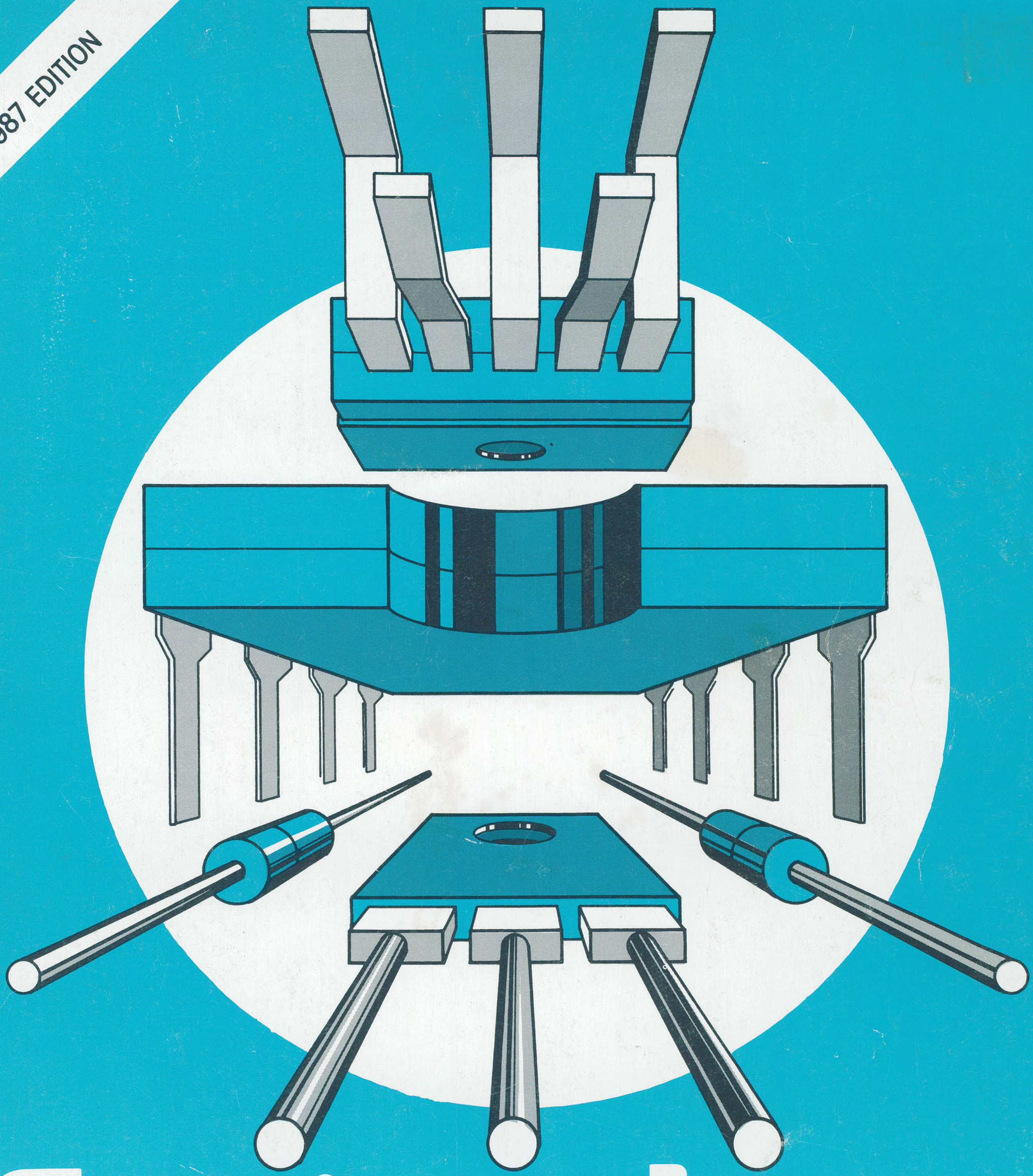
ARCHER®

Cat. No. 276-4010

1987 EDITION



Semiconductor Reference Guide

INCLUDES OVER 115,000 SEMICONDUCTOR SUBSTITUTIONS

INTEGRATED CIRCUITS INDEX BY GENERIC NUMBER

INTEGRATED CIRCUITS INDEX BY CATALOG NUMBER

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INTRODUCTION

This SEMICONDUCTOR REFERENCE HANDBOOK is intended to be just that—a reference handbook. It is not a definitive text book on semiconductors. It is a compilation of data on Radio Shack's line of prime-quality ARCHER semiconductors. Every ARCHER device covered in this Handbook is guaranteed prime—they are not "fall-outs" or "seconds"; all are top-quality, with known JEDEC, EIA or manufacturer's numbers.

At the back of the book is a cross-reference listing for replacement of Transistors, Diodes and other interchangeable semiconductor devices. The total number of cross-referenced devices exceeds 115,000. These cross-reference/replacement listings are computer-selected and are based on careful analysis of important parameters of the listed devices.

NOTE: If you can't find a replacement listing for a device you require, refer to the specification listings of the appropriate ARCHER family device. Often you will be able to make suitable replacements based on the information presented.

Each ARCHER replacement should meet or exceed the required parameters. However, due to differences in Quality Control and Manufacturing procedures (which often allow for or result in broad parameter variations), and because many of the ARCHER devices are capable of better performance than the original, Radio Shack does not guarantee, nor does it imply, that the listed items will provide an exact replacement in **every** instance. Therefore we recommend that you check the voltage and current requirements of the circuit (and other pertinent specifications) before replacement and compare with the specifications listed for that particular ARCHER device.

HOW TO USE THIS BOOK

This book has been prepared to aid in BOTH replacement and original applications of Semiconductor devices. The information included will be invaluable for the service technician as well as the circuit designer (whether he be an engineer, hobbyist, student or electronics experimeter).

We have included hints on handling Semiconductor devices, operating considerations, and some simple tests to aid you in evaluating the quality of the device in existing equipment (and thus the need for replacement). Also, a complete section on the specifications for each of the ARCHER devices is included; if there is any question in your mind about replacement equivalents or original use, refer to the appropriate category in the book. You will find the important characteristics specified there.

The next to last section is an extensive listing of replacement and cross reference between other manufacturer's numbers (both JEDEC/EIA 2N—numbers and in-house designations) and the ARCHER devices. This listing provides for the substitution of over 115,000 semiconductors with ARCHER devices.

The final section includes case style drawings and some handy reference notes, a comprehensive glossary of commonly used words, plus symbols and abbreviations.

CARE AND HANDLING OF TRANSISTORS

Most modern transistors are somewhat immune from mechanical shock; however, it is always a good idea to keep them from excessive mechanical shocks, especially the metal-case type (avoid dropping, etc).

When cutting transistor leads, use scissor-type cutting tools (rather than diagonal cutting tools which use a crimping action). Crimp-type cutting tools produce a mechanical shock along the lead which when transmitted to the semiconductor chip or material can cause fracture. Consider the force with which the cut lead flies off the crimp-type cutting tool and you have a good idea of the intensity of the equal and opposite force which acts on the lead going into the device.

It is always a good practice to use a heat-sink tool on a transistor lead when soldering (use a low-wattage iron—30-watts or less). Heat from soldering can cause problems (especially with certain types of semiconductor devices). Thus, to be sure, always use a heat-sink on the lead when soldering. Gripping the lead with long nose pliers between the solder connection and the case of the device makes a good heat-sink; or use a tool designed for such use.

SILICON OR GERMANIUM?

The quickest way to determine if a transistor is germanium or silicon type, is to check the normal emitter-base voltage drop. With NPN devices, if the base is approximately 0.25 volts positive with respect to the emitter, it is a germanium type. If the voltage is about 0.65 volts, it is a silicon type. For PNP devices, the voltage will be the same value, but opposite in polarity (0.25 volts for germanium and 0.65 for silicon).

OPERATING CONSIDERATIONS

Before replacing an original-equipment device with the recommended Archer Type:

(A) Compare the lead or terminal arrangement of the Archer replacement device with the lead or ter-

minal arrangement of the original device. If these arrangements are different, and the original transistor is a "plug in" type, bend the leads of the ARCHER device so that the base, emitter and collector leads will mate with the original transistor leads. Trim the leads after soldering in place.

CAUTION: Be particularly careful about "pin-circle" and "in-line" lead break-out type transistors. Often one manufacturer makes a type with "in-line" leads, while another may make the same type with "pin-circle" configuration. **Doublecheck both the original and the replacement device before soldering or plugging in transistors.**

BOTTOM VIEW

PIN-CIRCLE IN-LINE

(B) Certain considerations are involved whenever an original equipment transistor is replaced by one having a different type designation. When an ARCHER series transistor is used to replace an original equipment device in an untuned amplifier stage operating at a low signal level such as the untuned RF-amplifier (antenna) stage of a radio receiver, or a low-level AF amplifier stage, it is generally unnecessary to make any circuit adjustment to assure proper performance of the equipment. However, when a replacement is made in a turned RF amplifier stage, it is always advisable to check the alignment of the associated tuned circuits to assure proper tracking and to achieve the required gain without loss of stability.

(C) When replacements are made in stages operating at relatively high power levels, such as Class A and Class B AF output stages of automobile radio receivers, phonographs and AF-amplifier systems, the transistor bias should be checked and adjusted, if necessary, to protect the ARCHER replacement transistors against excessive dissipation and to minimize distortion. Means for making adjustments are generally provided in the equipment, and the necessary instructions are usually given in the equipment manufacturer's service data.

(D) When installing an ARCHER transistor as a substitute for an original equipment type in an FM tuner, TV tuner, or other circuits operating at frequencies in the VHF or UHF regions, it is extremely important not to change any of the lead lengths or position of the original circuit. Before removing the original transistor, carefully note its position with respect to other circuit components as well as the lengths and placement of the transistor leads, and duplicate these details as closely as possible with the ARCHER replacement transistor. Failure to observe this precaution can result in improper tuning or circuit instability. The same holds true for any replacement of Integrated Circuits, specially in FM radios and TV Receivers. Failure to observe this precaution can result in damage in the device. Transistor substitution in tuned circuits will often require realignment of the circuit.

SILICON VS SELENIUM RECTIFIERS

Silicon rectifiers are inherently more efficient than selenium or other metallic-oxide type rectifiers. When a silicon rectifier is used to replace a selenium rectifier in the power supply of a typical line-operated radio or TV receiver, the silicon rectifier will frequently deliver higher DC output voltage than the original device.

In some cases, this higher supply voltage may improve the performance of the equipment. However, in many other cases, it may immediately or eventually damage filter capacitors and/or other components which were designed to withstand only the voltage delivered by the original selenium rectifier. To prevent such damage, it is generally advisable to insert a power type resistor in series with the silicon rectifier either on the input side, between the AC supply and the rectifier, or on the output side between the rectifier and the first filter capacitor. The value of this resistor will depend on the required reduction in the DC output voltage and on the DC load current of the equipment. This value may be determined experimentally or calculated from the equation:

$$R = \frac{E}{I}$$

where R is the required resistance in ohms, E the required reduction in DC output voltage in volts and I the DC load current in amperes.

The wattage rating of the resistor should be at least 2 X EI (in no case less than 10 watts).

SOLDERING PRECAUTIONS

Extreme care should always be used in making solder connections to semiconductors. Momentary application of excessive heat, or even prolonged application of a properly heated soldering tool to a semiconductor lead or terminal, can permanently damage the device. Observe the following precautions in soldering a semiconductor lead or terminal:

1. Solder as far as possible from the body of the semiconductor.
2. Never, apply heat or molten solder to a lead or terminal for longer than 10 seconds or at a point closer than 1/16 inch to the body of the device.
3. Use a low voltage iron (30 watts or less) specifically intended for use with transistors or miniature circuit components.
4. Keep the surfaces to be soldered clean and the tip of the soldering tool adequately tinned so that the connection can be made as quickly as possible.
5. Always use a heat sink on the lead when soldering. Gripping the lead or terminal with longnose pliers between the solder connection and case or body allows the pliers to act as a heat sink, conducting heat away from the internal elements of the device.

ABOUT CASE DIMENSIONS

In some instances, the case of an ARCHER Semi-

conductor may be slightly taller or thicker than that of the original device or have a slightly different shape, particularly if the original device is a foreign type not made to U.S.A. EIA (JEDEC) standards. These mechanical differences should not affect the performance of the equipment in which the replacement is made and normally will not prevent or complicate the installation of the ARCHER replacement device.

You should realize that cross-reference substitution listings are created based **on electrical parameters (not necessarily on mechanical size or type).** Thus, when you make substitutions based on our listings, check for physical/mechanical compatibility. If space is limited, it would be a good idea to check physical dimensions as well as electrical specs before making substitution.

GENERAL PRECAUTIONS

ARCHER transistor and ARCHER semiconductors should not be inserted or withdrawn from circuits with the power on, because transient currents may cause permanent damage to the device. In some cases ARCHER semiconductors are in metal cans and thus could possibly become shock hazards if they are allowed to operate at a voltage appreciably above or below ground potential.

For the most effective protection, a power transistor should be operated with an adequate heat sink and with the lowest value of resistance or impedance in the emitter-to-base circuit consistent with driving signal considerations. The transistor should be protected against extremely high collector voltage pulses which may be generated when the device is operated with inductive loads particularly when current transients are present.

When replacing a power transistor or rectifier which is attached to the equipment chassis, or to a special heat sink, observe the following precautions:

A. In the case of oxide coated metal washers or wafers, which are frequently used as electrical insulators between the cases of power transistors and the chassis or heat sink, it is important not to scratch, chip or otherwise damage the oxide surface.

B. When installing an ARCHER power transistor, where a mica or oxide coated metal washer was used to insulate the case of the original device electrically from the case, apply a thin coating of Heat Sink Compound (Radio Shack Number 276-1372) between the washer and the chassis or heat sink.

TESTING A TRANSISTOR

Before replacing a transistor you want to be sure it needs to be replaced. Always check the entire circuitry to be sure the transistor requires replacement.

The best method for checking transistors is to use a good transistor checker (dynamic in-circuit and out-of-circuit type). However, a sensitive VOM can give you a good indication of the quality of the device.

I. In-Circuit Testing

A. First, check to see if the emitter-base junction is forward-biased. An NPN transistor should show the base 0.2 to 0.65 volts positive with respect to the emitter (approximately 0.25 volts for a germanium type and 0.6 volts for silicon). A PNP transistor should show the base 0.2 to 0.65 volts negative with respect to the emitter (0.25 volts for germanium and 0.6 volts for silicon).

B. Check to see if the device is functioning as an amplifier. Short the emitter-base junction to remove forward bias. Voltage at the collector lead should rise to approximately the potential of the collector supply buss line. Any difference is caused by I_{CES} (collector-to-base leakage current). The closer the collector voltage approaches the buss line, the lower I_{CES} is and the better the transistor.

II. Out-of-Circuit Testing

Again, for the best indication of transistor quality, use a good transistor checker. However, an ohmmeter can be used as described here.

Before using the ohmmeter, find out which polarity of the internal ohmmeter battery is connected to which test lead (not all ohmmeters have the + battery polarity connected to the red lead and the − battery polarity connected to the black lead). To determine the polarity of the leads when using the ohmmeter function, use an external voltmeter or study the schematic of your VOM.

Also, remember that in most transistor circuits you are dealing with low voltages and currents (in some cases, very low). Therefore, **NEVER** use RX1 scale (extensive currents can flow through a junction, permanently damaging the transistor). It is best to determine the maximum amount of current available in each resistance range before using an ohmmeter for testing semiconductor junctions.

After you have evaluated your VOM for the above and are sure you will not damage a transistor (with excessive current or voltage in any given ohmmeter range), proceed as follows:

A. Small Signal PNP Germanium Transistors
   1. Connect the positive lead of your ohmmeter to the emitter. Connect the negative lead to the base. You should read 200-500 ohms.
   2. Connect the negative lead to the collector. You should read 10K-100K. Shorting collector base, the resistance should decrease.

B. Small Signal NPN Germanium Transistors
   Reverse the polarity of the leads; the readings should be approximately the same.

C. Power PNP Germanium Transistors
   1. Connect the positive lead to the emitter. Connect the negative lead to the base. The reading should be 35-50 ohms.
   2. Connect the negative lead to the collector The reading should be several hundred ohms. Shorting collector to base, the resistance should decrease.

D. Power NPN Germanium Transistors
   Reverse the polarity of the leads; the reading should be approximately the same.

E. Small Signal PNP Silicon Transistors
   1. Connect the positive lead to the emitter. Connect the negative lead to the base. The reading should be 1K-3K.
   2. Connect the negative lead to the collector. The reading should be very high (may show as an "open").

F. Small Signal NPN Silicon Transistors
   Reverse the polarity of the leads; the readings should be approximately the same.

G. Power PNP Silicon Transistors
   1. Connect the positive lead to the emitter. Connect the negative lead to the base. The reading should be 200-1K.
   2. Connect the negative lead to the collector. The reading should be about 1 megohm or more.

H. Power NPN Silicon Transistors
   Reverse the polarity of the leads; the readings should be approximately the same.

The resistance readings noted above can only be approximate; as long as you obtain somewhat **proportionate** readings (emitter-base readings as compared to emitter-collector), you can safely assume the transistor is OK.

HANDLING OF INTEGRATED CIRCUITS

Because MOS devices have extremely high input resistance, they are susceptible to damage when exposed to static electrical charges (even electrical charges that normally build up on the human body can cause damage). To avoid possible damage to the devices during handling, testing, or actual operation, the following procedures should be observed:

1. Except when being tested or in actual operation, the leads of devices should be in contact with a conductive material, to avoid build-up of static charge.
2. Soldering iron tips, tools, metal parts of fixtures and handling facilities should be grounded.
3. Transient voltages may cause permanent damage to the device if it is removed or inserted with the power on.
4. Do not apply signals to the input with the power supply off.
5. All unused input leads must be connected to either V_{SS} or V_{DD} (whichever is appropriate for the logic circuit involved).

DIODES AND RECTIFIERS

GENERAL PURPOSE DIODES RATINGS @ 25°C

Catalog Number	PIV (min) V	If A	Ir (max) @ Vr μA	Vf (max) @ If V	Case Style
276-1101	50	1.000	10	1.6	DO41
276-1102	200	1.000	10	1.6	DO41
276-1103	400	1.000	10	1.6	DO41
276-1104	600	1.000	10	1.6	DO41
276-1114	1000	2.500	200	1.0	A1vm
276-1122	75	0.010	250nA	1.0	A1
276-1123*	60	0.085	15	1.0	A1
276-1141	50	3.000	500	1.2	A3q
276-1143	200	3.000	500	1.2	A3q
276-1144	400	3.000	500	1.2	A3q
276-1165†	40	1.000	5mA	0.55	A1

*GERMANIUM
†SCHOTTKY

ZENER DIODES—1 Watt

Catalog Number	Vz Volts ±10%	Iz @ mA	Zz @ Iz ohms max	Case Style
276-565	5.1	49	7	DO41
276-561	6.2	41	2	DO41
276-562	9.1	25	7	DO41
276-563	12.0	21	9	DO41
276-564	15.0	17	14	DO41

BRIDGE RECTIFIERS

Catalog Number	PIV (min) V	If (max) A	Case Style
276-1146	50	4	M532a
276-1151	50	1.4	M548
276-1152	100	1.4	M548
276-1161	50	1	Y1
276-1171	100	4	M532a
276-1173	400	4	M532a
276-1180	50	6	M532a
276-1181	250	6	M532a
276-1184	50	15	—
276-1185	50	25	—

BIPOLAR TRANSISTORS

Catalog Number	Direct Commercial Equivalent	Mat.	Appl.	Polarity	Power Diss. @25°C Free Air	f_T Typical MHz	V_{CBO} V	V_{CEO} V	V_{EBO} V	I_C Max	I_B Max	h_{FE}	@V_{CE} V	@ I_C mA	I_{CBO} at max V_{CB}	Case Style
276-1603#	2N3904	S	G.P.	NPN	350mW	300	60	40	6	200mA	—	40	1	0.1	—	T092
276-1604#	2N3906	S	G.P.	PNP	350mW	250	40	40	5	200mA	—	60	1	0.1	—	T092
276-1617#	2N2222	S	G.P.	NPN	500mW	250	60	30	5	800mA	—	35	10	0.1	—	T018
276-2007	2N1305	G	S	PNP	150nW	5	30	—	25	300mA	—	40	1	10	6μA	T05
276-2009	MPS2222A	S	G.P.	NPN	625mW	300	75	40	6	800mA	—	50	10	1	10nA	T092
276-2016	MPS3904	S	S	NPN	625mW	300	60	40	6	200mA	—	100–300	10	1	50nA	T092
276-2017	TIP31	S	P	NPN	40W‡	3	40	40	5	3A	1A	10–50	4	3A	300μA	T0220AB-2
276-2020	TIP3055	S	P	NPN	90W‡	3	100	70	7	15A	7A	20–70	4	4A	1mA	T0220
276-2023	MPS2907	S	S	PNP	625mW	200	60	40	5	600mA	—	50	10	1	20nA	T092
276-2027	MJE34	S	P	PNP	90W‡	3	40	40	5	10A	3A	20–100	4	3A	220μA	T0220
276-2030	2N3053	S	P	NPN	5W	100	60	40	5	700mA	—	50–250	10	150	—	T039
276-2041	2N3055	S	P	NPN	115W‡	2.5	100	60	7	15A	7A	20–70	4	1A	—	T03
276-2043	MJ2955	S	P	PNP	150W‡	4	100	60	7	15A	7A	70	10	0.5	0.7mA	T03
276-2055	2SC1308	S	SW	NPN	50W‡	—	1500	400	6	7A	0.8A	3	2	4A	100μA	T03
276-2058	2N4401	S	G.P.	NPN	625mW	250 min.	40	60	6	600mA	—	500	10	1	0.1μA	T092
276-2068	TIP120	S	P*	NPN	65W‡	0.1	60	60	5	5A	120mA	2500	3	500	0.2mA	T0220AB-2

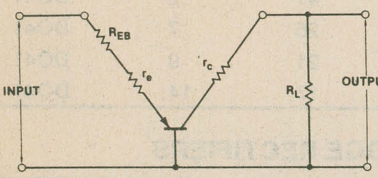
NOTE: All ratings given are for 25°C except where otherwise noted. #—Archer-Pack ‡With heat sink

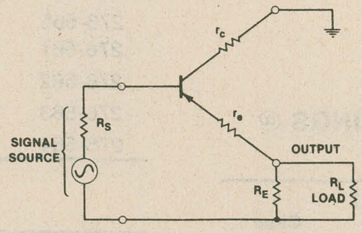
MATERIAL:
S—Silicon; G—Germanium

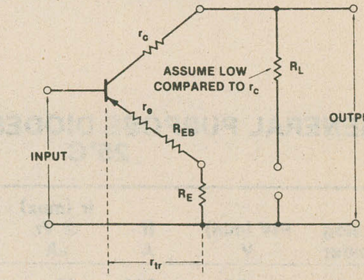
APPLICATION:

S—Switch
G.P.—General Purpose
P—Power amp/switch
RF/IF—RF/IF frequency
*—High Gain Darlington
UHF—Ultrahigh frequency
LL—Low Level
SW—TV Sweep

USEFUL INFORMATION







Parameters of Common-Base Circuit

Input Impedance $Z_{in} = r_{tr}$

Load Impedance $Z_L = R_L$ in parallel with input impedance of following stage.

Current Gain $A_i = \alpha = \dfrac{\beta}{1 + \beta}$

(In practice, α is 0.95 to 0.995, or approximately 1.)

Voltage Gain $A_v \approx \dfrac{Z_L}{r_{tr}} = g_m Z_L$

Parameters of Common-Collector Circuit

Input Impedance $Z_{in} = (\beta + 1)Z_L$
where,
Z_L is R_L in parallel with R_E.

Output Impedance $Z_{out} = \dfrac{R_s}{\beta+1}$
where,
R_s is the output impedance of the signal source.

Current Amplification $A_i \approx \beta$

Voltage Amplification A_v = Less than unity

Parameters of Common-Emitter Circuit

Input Impedance $Z_{in} = h_{fe} r_{tr}$

Load Impedance $Z_L = R_L$ in parallel with input impedance of next stage.

Current Gain $A_i = \dfrac{\Delta I_C}{\Delta I_B} = h_{fe}$
where,
$h_{fe} = \beta = \dfrac{I_c}{I_b} = \dfrac{\alpha}{1 - \alpha}$

Voltage Gain $A_v = \dfrac{\Delta V_C}{\Delta V_B} = \dfrac{Z_L}{r_{tr}} = g_m Z_L$

Power Gain $A_p = \dfrac{V_{out} I_{out}}{V_{in} I_{in}} = \beta \dfrac{Z_L}{r_{tr}}$

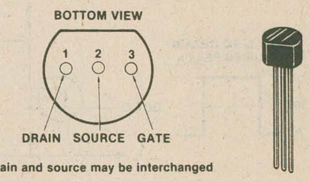
SILICON N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

MPF102
276-2062

GENERAL DESCRIPTION

The MPF102 is designed for small signal applications. These include VHF amplifiers and mixers.

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage	25 V
Drain-Gate Voltage	25 V
Gate-Source Voltage	25 V
Gate Current	10 mA
Total Device Dissipation	310 mW
Operating Junction Temperature	125°C
Storage Temperature Range	−65 to +150°C

N-CHANNEL MOSFET TRANSISTOR

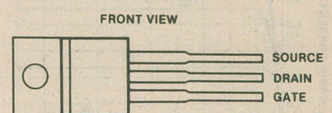
IRF511
276-2072

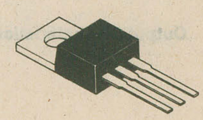
GENERAL DESCRIPTION

The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

This transistor also features all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

PIN CONNECTION





FEATURES

- Fast switching
- Low drive current
- Ease of paralleling
- No second breakdown
- Excellent temperature stability

APPLICATIONS

- Switching power supplies
- Motor controls
- Inverters
- Choppers
- Audio amplifiers
- High energy pulse circuits

ABSOLUTE MAXIMUM RATINGS

Drain-Source Voltage, V_{DS}	60V
Drain-Gate Voltage (R_{GS} = 1 MΩ), V_{DGR}	60V
Gate-Source Voltage, V_{GS}	±20V
Continuous Drain Current, I_D @ $T_C \cong 86°C$	3A
Pulsed Drain Current, I_{DM}	8A
Maximum Power Dissipation, P_D	20W
Linear Derating Factor	0.16W/K
Inductive Current, Clamped, I_{LM} (See Fig. 1) L = 100 μH	8A
Operating Temperature Range, T_J	−55 to +150°C
Storage Temperature Range, T_{stg}	−55 to +150°C

IRF511 276-2072

TEST CIRCUITS

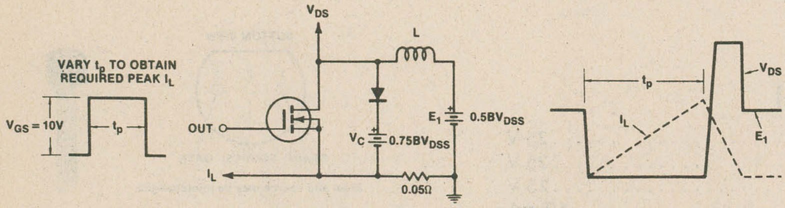


Figure 1—Clamped Inductive Test Circuit and Waveform

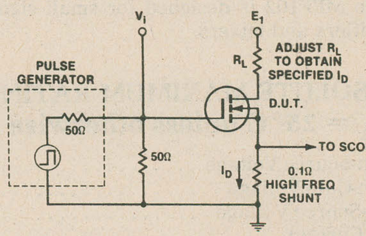
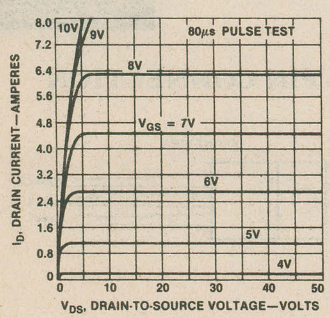
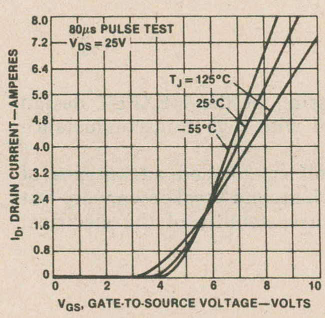


Figure 2—Switching Time Test Circuit

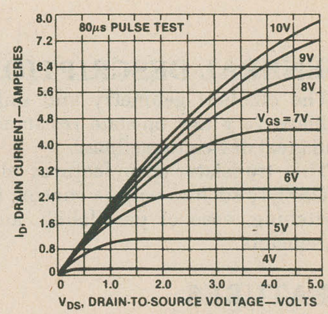
TYPICAL CHARACTERISTICS



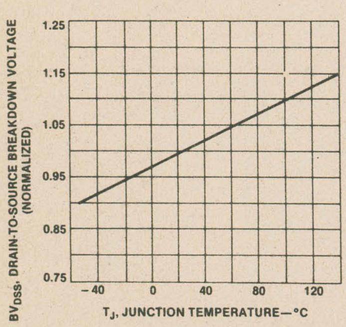
Output Characteristics



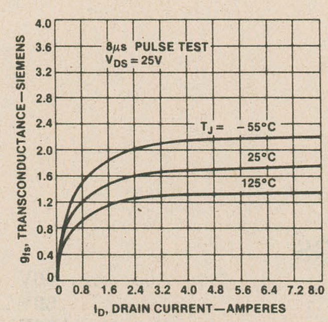
Transfer Characteristics



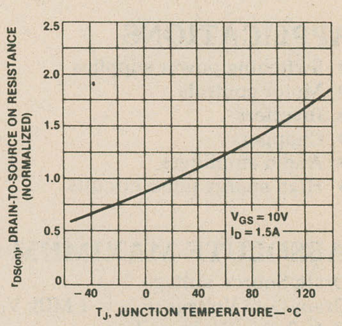
Saturation Characteristics



Breakdown Voltage vs Temperature



Transconductance vs Drain Current



Normalized On-Resistance vs Temperature

SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

2N3819
276-2035

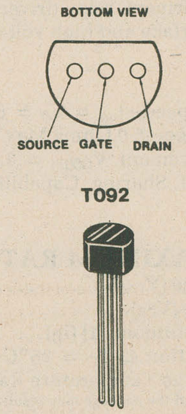
GENERAL DESCRIPTION

The 2N3819 is designed for general purpose small-signal applications. It features low capacitance between drain and gate terminals and an excellent high-frequency figure of merit. It achieves a low noise figure and good power gain with low crossmodulation and intermodulation.

ABSOLUTE MAXIMUM RATING
(T_A = 25°C unless otherwise noted)

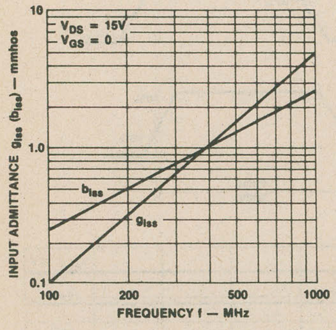
Gate-Source Breakdown Voltage BV_{GSS}	−40 V
Zero Gate Voltage Drain Current I_{DSS}	20 mA
Forward Transconductance g_{fs}	7.0− mmhos
Reverse Gate Leakage I_{GSS}	−100 pA
"ON" Resistance r_{DS}	500 ohms
Pinch Off Voltage $V_{GS(OFF)}$	−6.0 V
Output Conductance g_{os}	10 μmhos
Feedback Capacitance C_{rss}	0.9 pF
Input Capacitance C_{iss}	4.0 pF
Power Gain G_{PS}	12 dB
Power Dissipation	360 mW

PIN CONNECTION

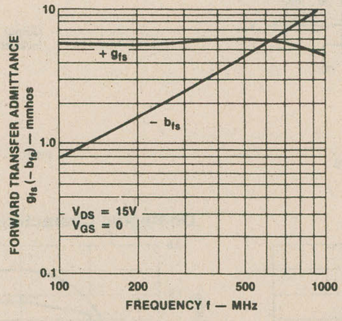


TYPICAL CHARACTERISTICS

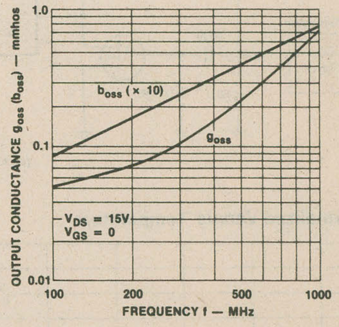
COMMON SOURCE



Input Admittance vs Frequency

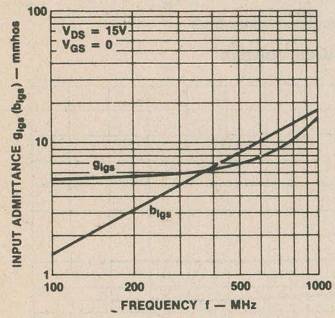


Forward Transfer Admittance vs Frequency

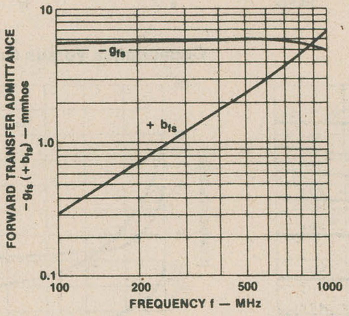


Output Conductance vs Frequency

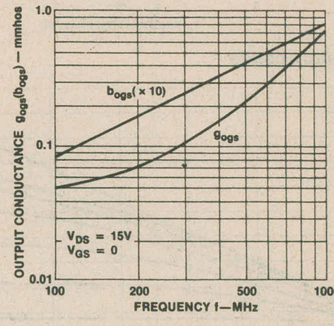
COMMON GATE



Input Admittance vs Frequency



Forward Transfer Admittance vs Frequency



Output Conductance vs Frequency

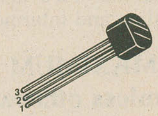
BS170
276-2074

N-CHANNEL TMOS FET

GENERAL DESCRIPTION

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL-to-high voltage interface and high voltage display drivers.

PIN CONNECTION



PIN 1. DRAIN
2. GATE
3. SOURCE

FEATURES

- Fast Switching Speed—$t_{on} = t_{off} = 6.0$ ns Typ
- Low On-Resistance—5.0 Ohms Max
- Low Drive Requirement, $V_{GS(th)} = 3.0$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

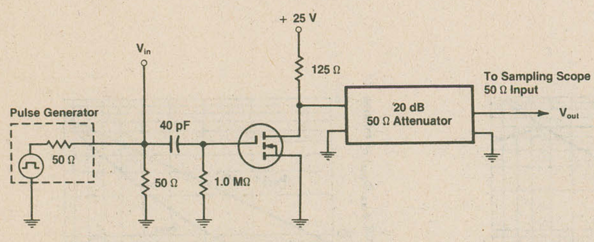
ABSOLUTE MAXIMUM RATINGS

Drain-Source Voltage (V_{DSS})	60 V
Gate-Source Voltage (V_{GS})	± 20 V
Drain Current—Continuous (1) (I_D)	0.5 A
Total Power Dissipation @ $T_C = 25°C$ (P_D)	0.83 W
Operating and Storage Temperature Range	− 55°C to + 150°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.

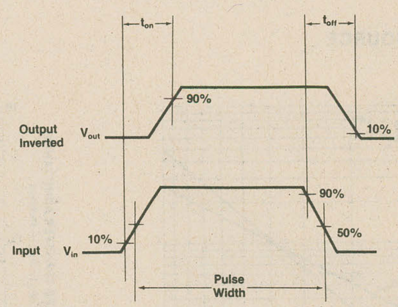
TYPICAL APPLICATIONS

Switching Test Circuit

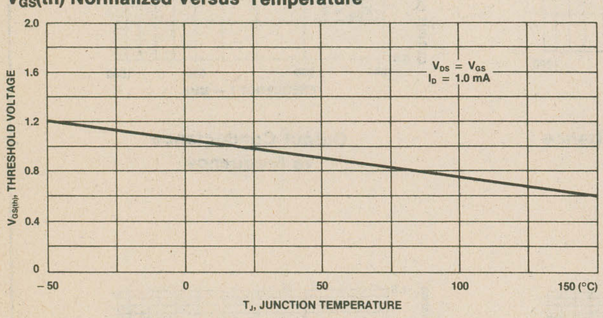


(V_{in} Amplitude 10 Volts)

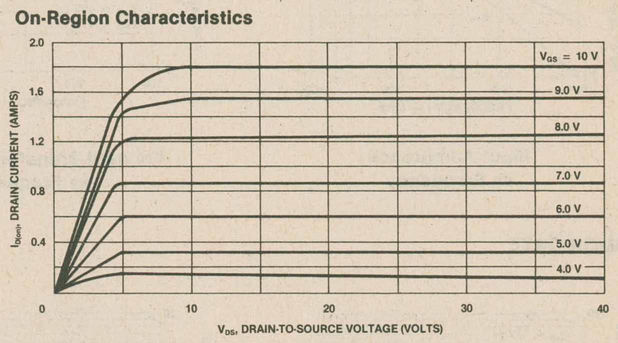
Switching Waveforms



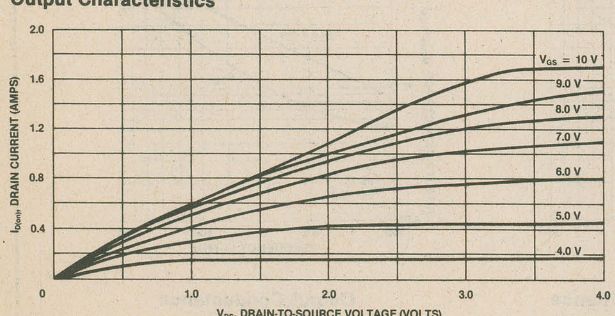
V_{GS}(th) Normalized Versus Temperature



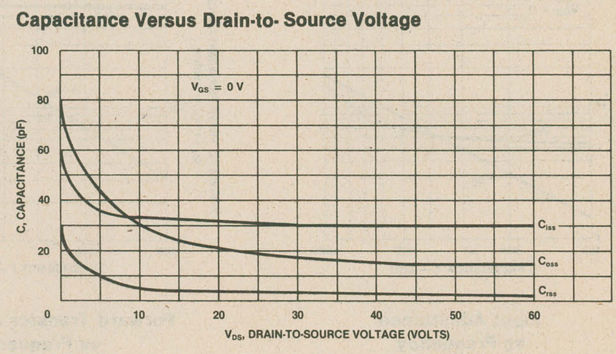
On-Region Characteristics



Output Characteristics



Capacitance Versus Drain-to- Source Voltage



TRANSIENT/SURGE ABSORBER

ERZ-C20DK201U
276-568
ERZ-C14DK201U
276-570

GENERAL DESCRIPTION

ZNR varistors are zinc oxide resistors whose resistance changes as a function of the applied voltage. The ZNR has a bilateral and symmetrical V-I characteristic curve and can therefore be used in circuits in place of back-to-back zener diodes. This gives your circuit clamping protection in either direction. The ZNR provides a highly reliable and economical way to protect against repeated high voltage transients and surges such as those produced by lightning, switching surges and noise spikes.

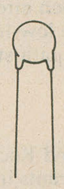
FEATURES

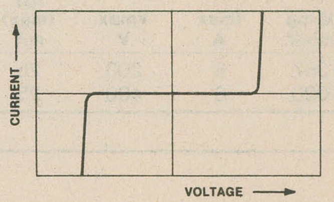
- Excellent clamping voltage characteristic and fast response time (< 50 nsec.) when subjected to impulse surges. Eliminates the discharge lag that is indicative of gap-type arrestors.
- Bilateral and symmetrical V-I characteristic curve. The ZNR can, therefore, be used both in AC and in DC circuits, for protection of either positive or negative transients.

ABSOLUTE MAXIMUM RATING

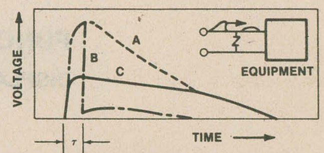
Varistor Voltage (V-I @ 1mA DD) (185V 225V)	200V
Applied Voltage AC_{RMS})	130V
(DC)	170V
Clamping Voltage @ Test Current (8 × 20 μsec) V_C(V)	340V
IP (A) (276-568)	100A
IP (A) (276-570)	50A
Peak Pulse Current (8 × 20 μs) 1 Time (276-568)	6500A
(276-570)	4500A
Energy (J) (276-568)	70J
(276-570)	35J
Power (276-568)	1W
(276-570)	0.60W
Capacitance (PF @ 1kHz) (276-568)	2000PF
(276-570)	1000PF
Operating Ambient Temperature	−40° + 85°C
Storage Temperature	−40° +125°C

PIN CONNECTION





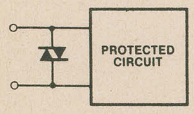
V-I Characteristic Curve



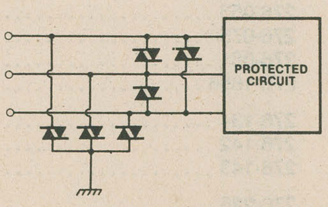
A: Original surge wave form
B: Clamping voltage using gap type arrestor
C: Clamping voltage using ZNR
τ: Discharge lag

Clamping Voltage Characteristics

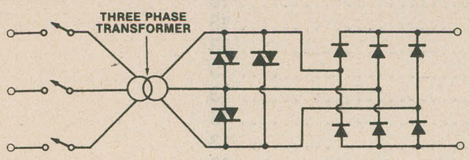
TYPICAL APPLICATIONS



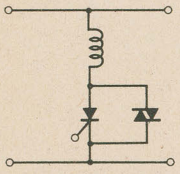
Single Phase Line Surge



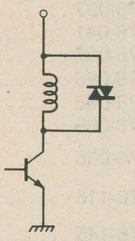
Three Phase Line Surge



Transformer Inductive Surge
by Primary Switch Off



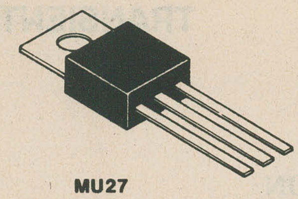
Solenoid Inductive Surge
by Thyristor Switching



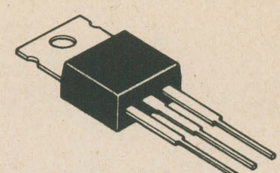
Solenoid Inductive Surge
by Transistor Switching

SPECIAL PURPOSE DEVICES (SCR) (TRIAC)

276-1000 276-1001 276-1020 276-1067 THYRISTORS



MU27



TO220AB

GENERAL DESCRIPTION

Thyristors and their trigger devices can take numerous forms, but they share these characteristics:

- They are "open circuits," capable of withstanding rated voltage until triggered.
- They become low-impedance current paths when triggered, and remain so, even after the trigger source is removed, until current through that path stops, or is reduced below a minimum "holding" level.

SCRs

Silicon-Controlled Rectifiers (SCRs) are Thyristors intended to switch load currents in one direction only, making them useful for DC and half-wave AC applications as well as full-wave applications, in which bidirectional current is routed in one direction through the SCR via a bridge rectifier.

Catalog Number	Imax A	Vmax V	I_{GT} (max) mA	V_{GT} (max) V	Case Style
276-1067	6	200	25	1.5	MU27
276-1020	6	400	25	1.5	MU27

TRIACs

Triacs are bidirectional Thyristors, in which a single trigger source turns the device on for load current in either direction. Because they do not require a bridge rectifier in order to handle full-wave AC, Triacs are useful in AC power applications that require full source power control capability to be applied to the load.

Catalog Number	Imax A	Vmax V	I_{GT} (max) mA	V_{GT} (max) V	Case Style
276-1001	6	200	50	2.5	TO220AB
276-1000	6	400	50	2.5	MU27

OPTOELECTRONIC INDEX BY FUNCTION

LED INDICATORS

Catalog Number	Direct Commercial Equivalent	Peak Wave Length nM	Color	Forward Voltage V_F (V)	Reverse Voltage V_R (V)	Max DC Forward Current I_F (MA)	Max Pwr Diss P_D (MW)	Fig. No.
276-018	PR5534S	700	RED	2.5	4	100	75	4
276-021	SLP-236B	565	YELLOW	2.8	3	30	70	5
276-022	SLP-236B	565	GREEN	2.8	3	30	70	5
276-025	R9-56	—	RED/GREEN	2.0	3.0	10	—	7
276-026	—	650	RED	—	3	50	100	2
276-033	TLR-147	700	RED	2.1	4	35	100	1
276-037	SLP-235B	565	GREEN	2.8	3	30	70	4
276-041	—	700	RED	1.75	3	70	140	3
276-065	369HHD	697	RED	1.8	5	20	75	8
276-066	ER300	660	RED	2.0	4	50	100	9
276-068	—	700	RED	1.9	—	30	—	6
276-069	—	560	GREEN	2.1	—	30	—	6

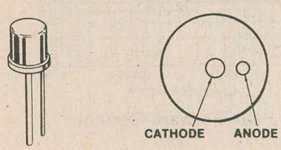


FIGURE 1
Miniature LED with diffused lens. This LED is compatible with most TTL and transistor circuits. It features a Fresnel lens design.

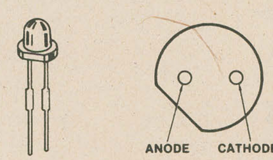


FIGURE 2
This LED features a frosted diffused lens in a plastic encapsulant. When the device is on, it appears as a large, soft light source, making it ideally suited for front panel applications.

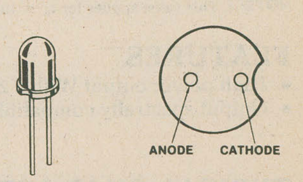


FIGURE 3
This device is a jumbo LED with a diffused lens. It can be used in applications such as pilot and indicator lamps.

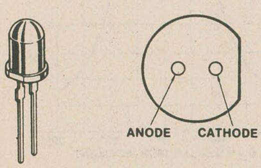


FIGURE 4
Subminiature LED with diffused lens. This device has solid state reliability and is compatible with most TTL and transistor circuits.

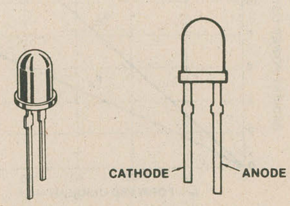


FIGURE 5
This is a frame type solid state LED with a diffused lens.

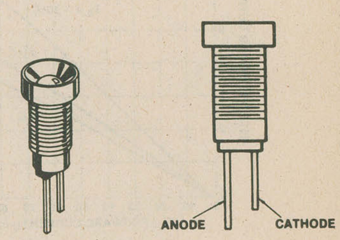


FIGURE 6
This is a subminiature LED indicator with polished chrome reflective holder.

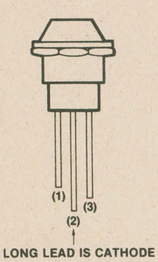


FIGURE 7
This is a three terminal LED. The light color radiates "red" when terminals 2 and 3 are used. Green light radiates when terminals 1 and 2 are used.

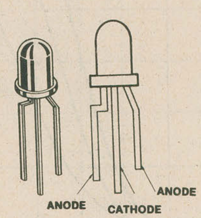


FIGURE 8
This is a round type red LED

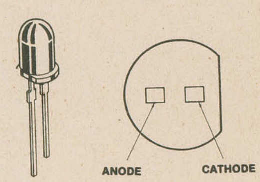


FIGURE 9
This is a high-brightness red LED with a clear lens.

TIL906-1
276-143

P-N GALLIUM ALUMINUM ARSENIDE INFRARED- EMITTING DIODE

GENERAL DESCRIPTION

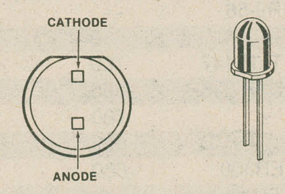
This is a P-N Gallium Aluminum Arsenide Infrared-Emitting diode designed to emit near infrared radiation when forward biased. Its output is spectrally compatible with silicon sensors and has a high power output with a 20° beam angle.

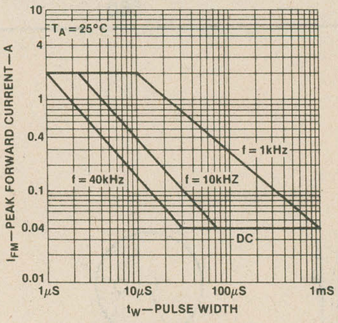
ABSOLUTE MAXIMUM RATINGS

Forward Voltage (Static) (VF) .... 1.75 V
Reverse Voltage (VA) .... 3 V
Continuous Forward Current at (Or Below)
25°C Free-Air Temperature .... 100 mA
Peak Forward Current (See Note 1) .... 2 A
Reverse Current (V_R = 3 V) .... 100 μA
Radiant Power Output (P_O) (IF = 20 mA) .... 1.5 MW
Emission Beam Angle Between
Half-Intensity Points .... 20°
Wave Length at Peak Emission (IF = 20 mA) .... 880 nM
Operating Temperature Range .... −40°C To 80°C
Storage Temperature Range .... −40°C to 100°C

NOTE: 1. This value applies for $t_w \leq 10\ \mu s$, $f \leq 1$ kHz. See Figure 1.

PIN CONNECTION





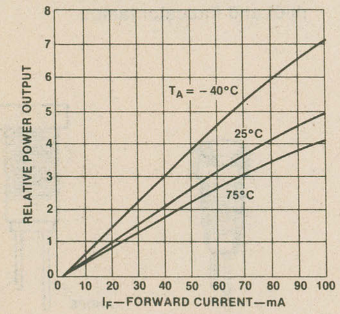
Peak Forward Current
vs
Pulse Width

Figure 1

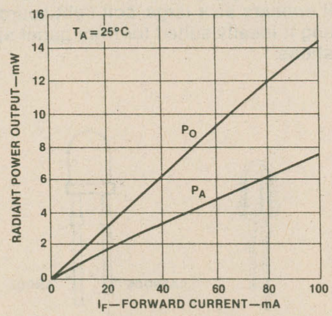
FEATURES

- High power output With a 20° beam angle
- Output spectrally compatible with silicon sensors

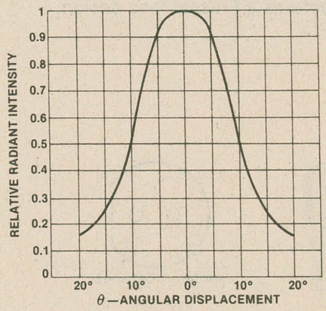
TYPICAL CHARACTERISTICS



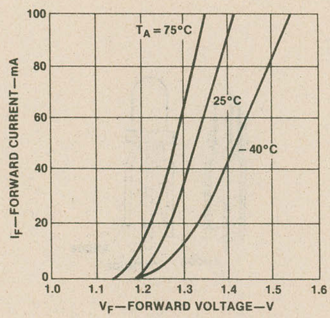
Relative Power Output
vs
Forward Current



Radiant Power Output
vs
Forward Current



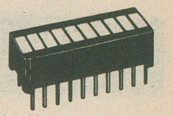
Relative Radiant Intensity
vs
Angular Displacement



Forward Conduction
Characteristics

B1001R
276-081

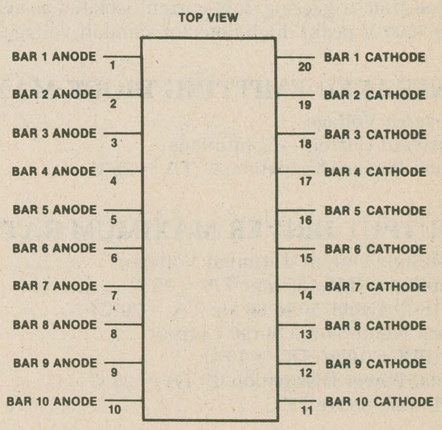
HIGH EFFICIENCY RED BAR GRAPH DISPLAY



GENERAL DESCRIPTION

The B1001R is a 10 segment bar graph display with separate anodes and cathodes for each light segment. The packages are end stackable.

PIN CONNECTION



FEATURES

- Large segments, closely spaced
- End stackable
- Fast switching, excellent for multiplexing
- Low power consumption
- Directly compatible with ICs
- Wide viewing angle

ABSOLUTE MAXIMUM RATINGS
(25°C Free Air Temperature Unless Otherwise Specified)

Power dissipation 100mW
Continuous forward current
  Total .... 300 mA
  Per segment .... 30 mA
Reverse voltage
  Per segment .... 5.0 V
Storage and operating temperature .... −30 to +80°C

ELECTRO-OPTICAL CHARACTERISTICS

Forward Voltage .... 1.6 V
Peak emission wavelength 655nm

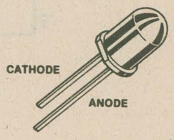
F336GD
276-030
F336HD
276-036

BLINKING LED

GENERAL DESCRIPTION

The F336GD is a solid state LED with a green diffused plastic lens. The F336HD is a solid state LED with a red diffused plastic lens. A built-in IC flashes the LEDs on/off and can be driven directly by standard TTL and CMOS circuits, eliminating the need for external switching circuitry.

PIN CONNECTION



FEATURES

- Built-in IC chip, flashes LED on and off to attract attention
- Pulse rate 1.0HZ
- T1 3/4 size
- Larger full flood radiating area
- 1-inch leads
- 1.2mcd @ V_F = 3.0V
- IC compatible

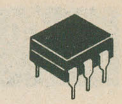
ABSOLUTE MAXIMUM RATINGS

Operating Voltage .... 5 V
Peak Inverse Voltage .... 0.4 V
Operating Temperature .... 0°C to 70°C
Storage Temperature .... −20°C to +85°C
Lead Soldering Temperature (1/16 inch from case) .... 5 sec. @ 260°C

ELECTRO-OPTICAL CHARACTERISTICS

Luminous Intensity .... 1.2 mcd
Emission Peak Wavelength (F336GD) 565nm
  (F336HD) 597nm
Spectral Line Halfwidth (F336GD) 30nm
  (F336HD) 90nm
Peak Current (50% Duty Cycle) .... 3.5 MA
Pulse Rate .... 2.0 HZ

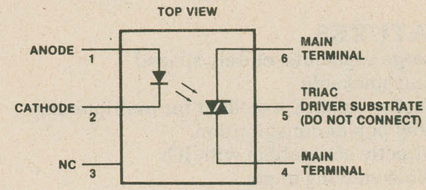
MOC3010 276-134 OPTOCOUPLER TRIAC DRIVER



GENERAL DESCRIPTION

This device consists of a gallium-arsenide infrared emitting diode, optically coupled to a silicon bilateral switch and is designed for applications requiring isolated triac triggering, low-current isolated ac switching, high electrical isolation (to 7500 V peak), high detector standoff voltage, small size, and low cost.

PIN CONNECTION



INFRARED EMITTING DIODE MAXIMUM RATINGS

Reverse Voltage	3.0 volts
Forward Current—Continuous	50 mA
Total Power Dissipation @ TA = 25°C	100 mW

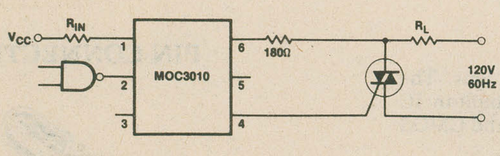
OUTPUT DRIVER MAXIMUM RATINGS

Off-State Output Terminal Voltage	250 Volts
On-State RMS Current TA = 25°C	100 mA
(Full Cycle, 50 to 60 Hz TA = 70°C)	50 mA
Peak Nonrepetive Surge Current	1.2 A
(PW = 10ms, DC = 10%)	
Total Power Dissipation @ TA = 25°C	300 mW
Derate above 25°C	4.0 mW/°C

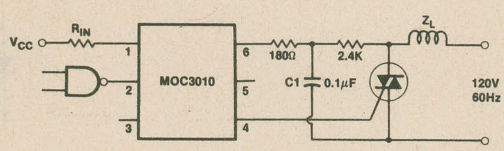
TOTAL DEVICE MAXIMUM RATINGS

Isolation Surge Voltage (1s)	7500 Vac
(Peak ac Voltage, 60 Hz, 5 Second Duration)	
Total Power Dissipation	330 mW
Junction Temperature Range	−40 to +100°C
Ambient Operating Temperature Range	−40 to +70°C
Storage Temperature Range	−40 to +150°C
Soldering Temperature (10s)	260°C

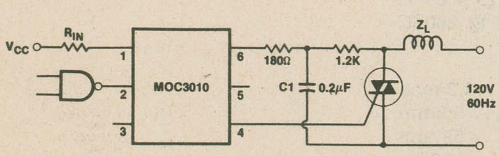
APPLICATIONS



Resistive Load

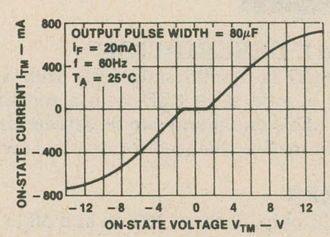


Inductive Load with Sensitive Gate Triac ($I_{GT} \leq 15mA$)

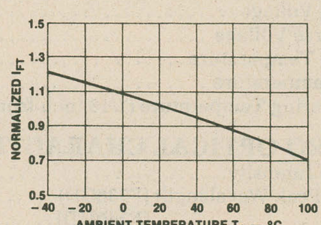


Inductive Load with Non-Sensitive Gate Triac ($15mA < I_{GT} < 50mA$)

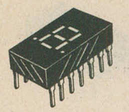
TYPICAL CHARACTERISTICS



On-State Current vs On-State Voltage



Trigger Current vs Temperature



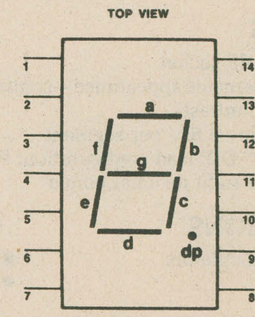
COMMON CATHODE DISPLAY

MAN74
276-075

GENERAL DESCRIPTION

This is a red .3 inch common cathode RHDP Display device with a brightness or luminous intensity (Per Seq. MIN) of 125 μcd @ 10mA.

PIN CONNECTION

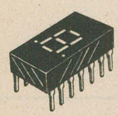


APPLICATIONS

- Instruments
- Test Equipment
- Office Machines
- Computers
- Automobiles
- Clocks/Radios
- Communication Equipment
- Calculators
- CB Radios

ABSOLUTE MAXIMUM RATINGS

Forward Voltage .... 2 V
Forward Current .... 20 mA
Power (P_D) .... 700 mW
Wave Length .... 660 nM
Brightness/Luminous Intensity @ 10mA .... 125 μcd



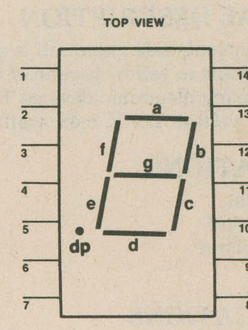
LED DISPLAY

276-1656

GENERAL DESCRIPTION

This is a 0.4'' common anode 7-segment display. Left Decimal 14 PIN DIP

PIN CONNECTION



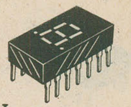
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage Per Segment or D.P (VR) 6.0V
Forward Voltage, Any Segment or D.P (VF) IF = 20mA 2.0V
Continuous Forward Current Per Segment or D.P 25mA
Peak Forward Current Per Segment or D.P ($t \leq 10$ μsec) 400mA
Power Dissipation Per Segment or D.P 50mW
Peak Wavelength (λ Peak) 655NM
Operating Temperature .... −35 to +85°C
Storage Temperature .... −40 to +85°C

COMMON ANODE

PIN	FUNCTION
1	CATHODE a
2	CATHODE f
3	ANODE
4	NO PIN
5	NO PIN
6	CATHODE dp
7	CATHODE e
8	CATHODE d
9	NO CONNECTION
10	CATHODE c
11	CATHODE g
12	NO PIN
13	CATHODE b
14	ANODE

276-053 0.3" SOLID STATE SEVEN SEGMENT DISPLAY



GENERAL DESCRIPTION

The 276-053 is a common anode LED numeric display. The large 0.3" high character size generates a bright, continuously uniform 7 segment display. Designed for viewing distances of up to 10 feet, this single digit display has been human engineered to provide a high contrast ratio and wide viewing angle.

FEATURES

- Fits 14 pin DIP socket
- Excellent character appearance—continuous uniform segments; wide viewing angle; high contrast
- IC compatible—1.6 V per segment
- Standard 0.3" DIP lead configuration; PC board or standard socket mountable
- Both left and right decimal points

APPLICATIONS

- Electronic calculators
- TVs
- Radios
- Frequency counters
- Digital clocks

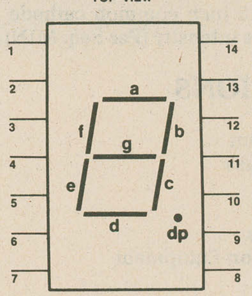
RADIANT CHARACTERISTICS (IF=20mA) T_A=25°C

Luminous Intensity .... 250 mcd
Wavelength (Peak) .... 655 nM

ABSOLUTE MAXIMUM RATINGS

Power Dissipation T_A=25°C .... 400 mW
Average Forward Current/Segment or Decimal Pt. T_A =25°C .... 25 mA
Peak Forward Current/Segment or Decimal Pt. T_A=12°C
(Pulse Duration 500μs) .... 150 mA
Reverse Voltage per Segment or Decimal Pt. .... 6 V
Operating Temperature Range .... −20 to +85°C
Storage Temperature Range .... −20 to +85°C
Max Solder Temperature 1/16" Below Seating Plane (t ≤ 5 sec.) .... 230°C

PIN CONNECTION



COMMON ANODE

PIN	FUNCTION
1	CATHODE a
2	CATHODE f
3	ANODE
4	NO PIN
5	NO PIN
6	CATHODE dp
7	CATHODE e
8	CATHODE d
9	NO CONNECTION
10	CATHODE c
11	CATHODE g
12	NO PIN
13	CATHODE b
14	ANODE

ALTERNATE CONNECTION

PIN	FUNCTION
1	NO PIN
2	ANODE
3	CATHODE-f
4	CATHODE-g
5	CATHODE-e
6	CATHODE-d
7	NO PIN
8	NO PIN
9	ANODE
10	CATHODE-dp
11	CATHODE-c
12	CATHODE-b
13	CATHODE-a
14	NO PIN

276-116 CADMIUM SULPHIDE PHOTOCELL

GENERAL DESCRIPTION

A cadmium sulphide photo cell is a light variable resistor which is most sensitive in the green to yellow portion of the light spectrum. With it you can use light to control many electronic devices. Max. resistance .5 meg., min. resistance 100 ohms, max. voltage 170 V, max. wattage .2 watts, rugged epoxy case.

APPLICATIONS

- Night light
- Light control
- Burglar alarm
- Relay

SPECIFICATIONS

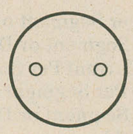
- Shape .... Round
- Sensitive Area .... .07 sq. in.
- Weight .... 1.56 gms.
- Resistance at 1 Ftc (2870°K) .... 1.7k Ohms . 40%
- Typical Resistance 100 Ftc (2870°K) .... 100 Ohms
- Resistance Dark Minimum (1 Minute) .... 0.5 Megohms

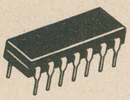
ABSOLUTE MAXIMUM RATINGS

Max. Applied Voltage (ac or dc) .... 170 V peak
Max. Power Dissipation at 25°C .... 2 watts
Power Derating .... Linearly to 0 @ 75°C
Operating Temp. Range .... −40 to +75°C

CONNECTIONS

BOTTOM VIEW





TRI-COLOR LIGHT EMITTING DIODE

XC-5491
276-035

GENERAL DESCRIPTION

The XC-5491 tri-state LED provides red, green, and yellow emission in the same package. This LED is a popular .200 diameter, two-leaded package containing a red and green LED chip in inverse parallel. By reversing the polarity of the applied current, the LED will emit red or green light while an AC voltage results in yellow light. The chips used in the XC-5491 are brightness matched so that the light output is uniform. This eliminates the necessity for the special drive circuits previously required with tri-state lamps.

These lamps provide the designer with the capability of efficiently displaying three functions with one indicator. This reduces the number of front panel indicators and simplifies design.

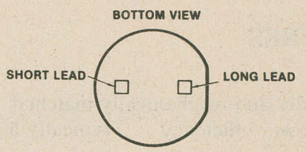
FEATURES

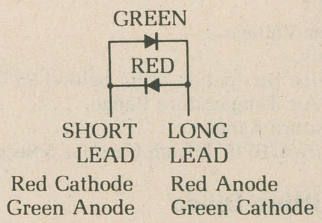
- 3 States—red, green, and yellow
- Equal brightness in all three colors
- Popular T 1¾ size package
- Wire wrappable leads

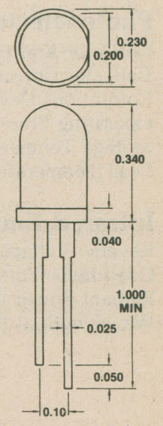
ABSOLUTE MAXIMUM RATINGS

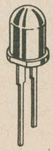
Forward Current	25 mA
Peak Reverse Voltage	5V
Power Dissipation	100 mW
Operating Temperature Range	−55 to +85°C
Lead Solder Temperature	260°C

PIN CONNECTION









INFRARED PHOTOTRANSISTOR

TIL414
276-145

GENERAL DESCRIPTION

The TIL414 is an NPN silicon phototransistor in A T-1 3/4 style case. It provides high speed and high photosensitivity, suitable for IR switching applications.

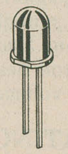
ABSOLUTE MAXIMUM RATINGS

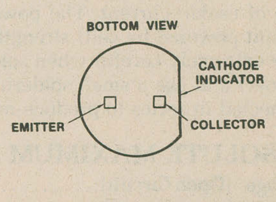
Collector-Emitter Voltage	50 V
Emitter-Collector Voltage	7 V
Power Dissipation	50 mW
Operating Temperature	−40° to +100°C

ELECTRICAL CHARACTERISTICS (Typical)

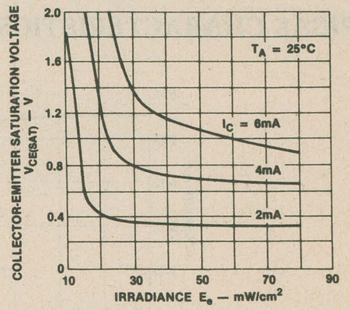
Dark Current (V_{CE} = 30 V)	25 nA
Light Current (V_{CE} = 5 V•E_e = 20mW/cm²)	7 mA
Collector-Emitter Saturation	0.4 V
Rise Time	8 μs
Fall Time	6 μs

PIN CONNECTION





TYPICAL CHARACTERISTICS



Collector-Emitter Saturation Voltage vs Irradiance

276-142 INFRARED EMITTER AND DETECTOR

GENERAL DESCRIPTION

The 276-142 is a pair consisting of an infrared photodetector and an infrared-emitting diode. The diode is capable of emitting radiant energy in the infrared region of the spectrum.

FEATURES

- Spectrally and mechanically matched
- High power efficiency . . . typically 5 percent at 25°C

ABSOLUTE MAXIMUM RATINGS

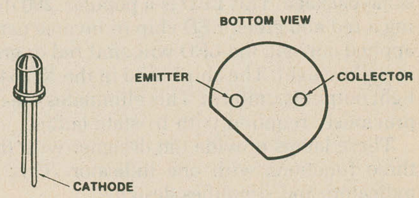
Photodetector

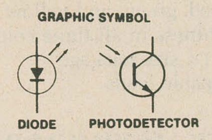
Collector-Emitter Voltage	20V
Collector Current	25mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature	50mW
Operating Free-Air Temperature Range	−40 to +80°C
Storage Temperature Range	−40 to +85°C
Lead Temperature 1/16 Inch from Case for 5 Seconds	240°C

Infrared-Emitting Diode

Reverse Voltage	2V
Continuous Forward Current	40mA
Radiant Power Output	0.5mW
Wavelength at Peak Emission	915mm

PIN CONNECTION





276-124 2.5×5cm SILICON SOLAR CELL

GENERAL DESCRIPTION

A solar cell is a silicon semiconductor device which converts light energy directly to electricity. A typical 2.5×5cm cell will produce 0.42 volt and up to .18 amp of usable current. The power generated is affected by the load resistance (circuit powered by cell) strength of sunlight and temperature.

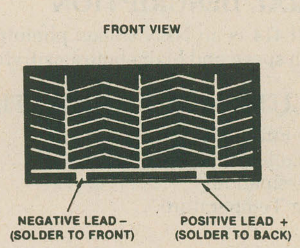
Be extremely careful when soldering leads. Use only a very fine wire (#26 or thinner) and use a small soldering iron (less than 50 watts). Solar cells may be connected in series to produce more voltage and in parallel for more current.

ABSOLUTE MAXIMUM RATINGS

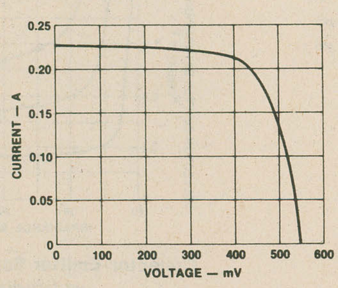
Voltage (Open Circuit):	0.55V
Current (short circuit):	0.2A

(Test conditions: Full sunlight at noon on a clear day at 25°C (76°F))

CONNECTIONS



TYPICAL CHARACTERISTICS



Current vs Voltage

INFRARED-EMITTING DIODE DETECTOR

MFOE71
MFOD72
276-225

GENERAL DESCRIPTION

The MFOE71 and MFOD72 Fiber Optic devices are designed for low cost, medium frequency, short distance systems using 1000 micron core plastic fiber.

FEATURES

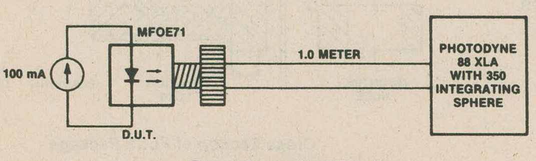
- Fast Response - > 10MHz (MFOE71)
- Standard Phototransistor (MFOD72)
- Spectral Response Matched to MFOE71, MFOD72
- Annular Passivated Structure for Stability and Reliability (MFOD72)
- Includes Connector
- Simple Fiber Termination and Connection (Cross Section of FLCS Package)
- Easy Board Mounting
- Molded Lens for Efficient Coupling

APPLICATIONS

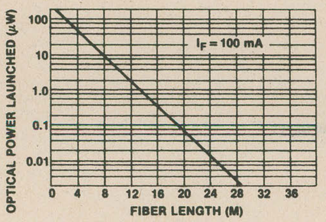
- High Isolation Interconnects
- Disposable Medical Electronics
- Coin operated machines
- Copy Machines
- Electronic Games
- Industrial Clothes Dryers

ABSOLUTE MAXIMUM RATINGS

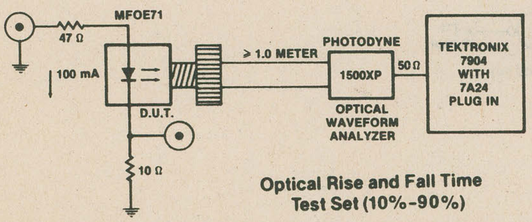
Reverse Voltage (VR) MFOE71	6.0V
Reverse Voltage (VR) MFOE71 (I_R = 100μA)	4.0V
Breakdown Voltage (Collector-Emitter) MFOD72	30V
Forward Voltage (VF) MFOE71	1.5V
Dark Current (Collector) (VCE = 10V) MFOD72	100nA
Forward Current (IF) MFOE71	150mA
Power Diss (PD)	150mW
Responsivity (V_{CC} = 5.0 Volts) (R) MFOD72	125μA/μW
Operating and Storage Temperature Range	−40 to +85°C



Power Launched Test Set

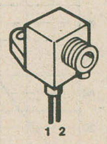


Power Launched (PL)
vs
Fiber Length

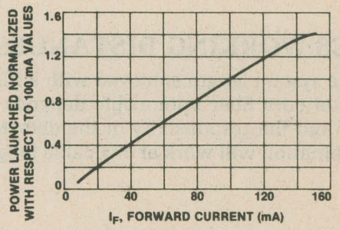


Optical Rise and Fall Time
Test Set (10%-90%)

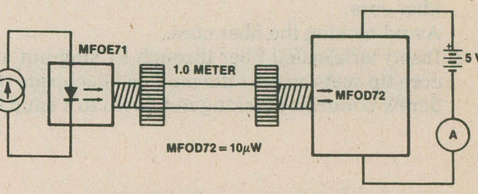
PIN CONNECTION



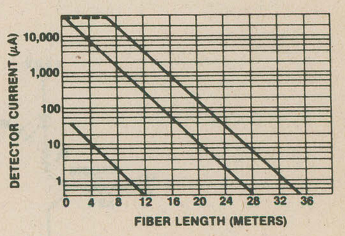
TYPICAL CHARACTERISTICS



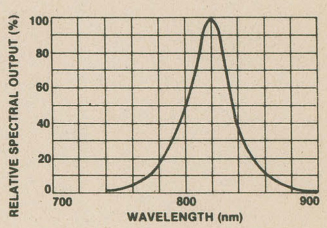
Normalized Power Launched
vs
Forward Current



Responsivity Test Configuration



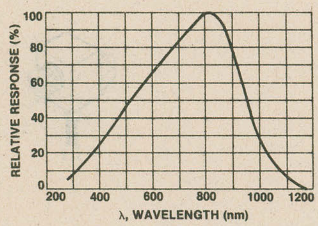
Detector Current
vs
Fiber Length



Typical Spectral Output
vs
Wavelength

MFOE71 MFOD72 276-225

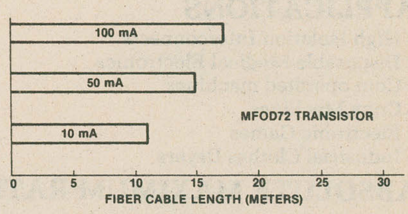
TYPICAL CHARACTERISTICS (Cont'd)



Relative Spectral Response

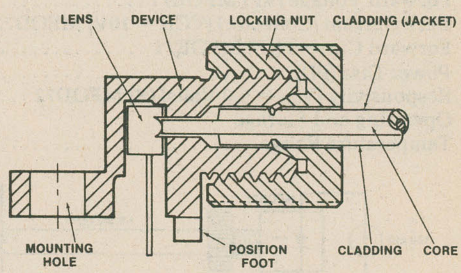
FLCS WORKING DISTANCES

The system length achieved with a FLCS emitter and detector using the 1000 micron core fiber optic cable depends upon the forward current through the LED and the responsivity of the detector chosen. The MFOE71 and MFOD72 combination will work at any cable length up to the maximum length shown.



Termination Instructions

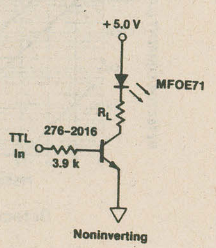
1. Cut cable squarely with sharp blade or hot knife.
2. Strip jacket back with 18 gauge wire stripper to expose 0.10-0.18″ of bare fiber core.
   Avoid nicking the fiber core.
3. Insert terminated fiber through locking nut and into the connector until the core tip seats against the molded lens inside the device package.
   Screw connector locking nut down to a snug fit, locking the fiber in place.



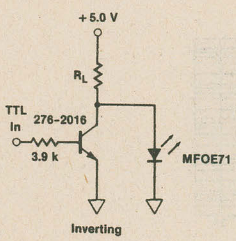
Cross Section of FLCS Package

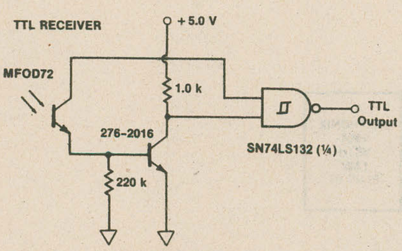
TYPICAL APPLICATIONS

TTL TRANSMITTERS

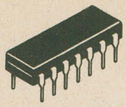


I_F	R_L
10 mA	330
50 mA	68
100 mA	33





5.0 kHz Transistor Receiver



QUAD TWO-INPUT NOR GATE

4001
276-2401

GENERAL DESCRIPTION

The 4001 quad 2-Input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FEATURES

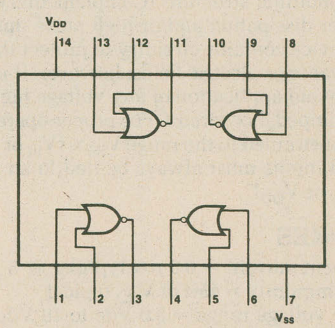
- Quiescent current = 0.5 nA typ/pkg @ 5 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode protection on all inputs
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Single supply operation—positive or negative
- High fanout > 50
- Input impedance = 10^{12} ohms typical
- Logic swing independent of fanout

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

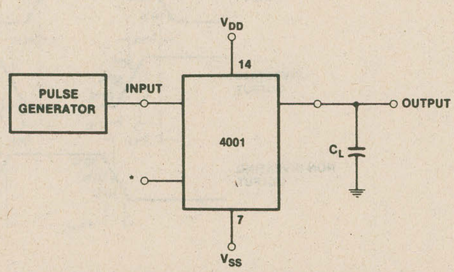
DC Supply Voltage	−0.5 to +16 Vdc
Input Voltage, All Inputs	−0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Pin	10 mAdc
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C

PIN CONNECTION

TOP VIEW

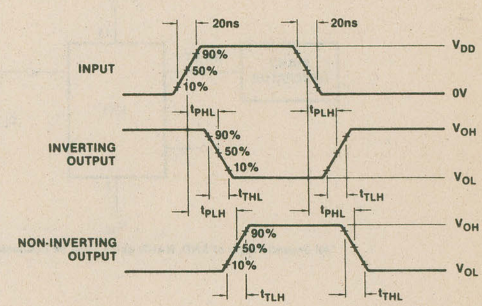


SWITCH TIME TEST CIRCUIT

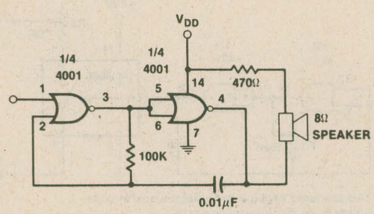


*All unused inputs of OR, NOR gates must be connected to V_{SS}.

SYNC TIMING WAVEFORMS

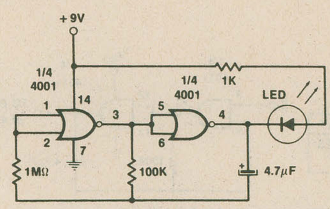


TYPICAL APPLICATIONS



Tone frequency is about 1kHz

Gated Tone Source



LED flashes 1-2 times/second

LED Flasher

4011 QUAD TWO-INPUT NAND GATE

276-2411

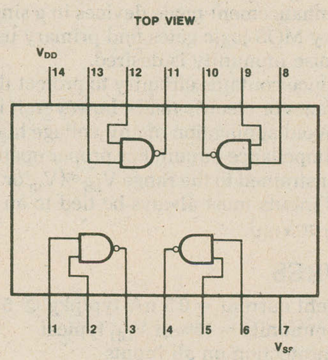
GENERAL DESCRIPTION

The 4011 is constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN CONNECTION



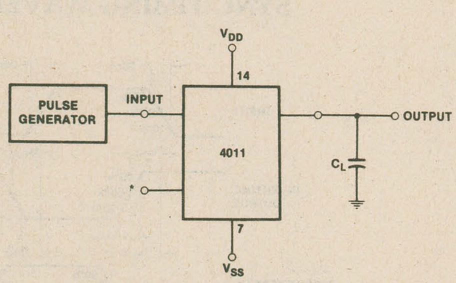
FEATURES

- Quiescent current = 0.5 nA typ/pkg @ 5 Vdc
- Noise immunity = 45% of V_{DD} typical
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Double diode protection on all inputs

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

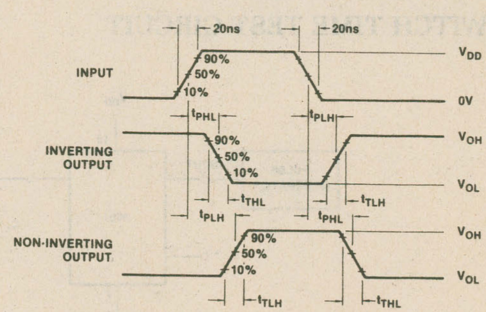
DC Supply .... −0.5 to +16 Vdc
Input voltage, All Inputs .... − 0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Pin .... 10 mAdc
Operating Temperature Range .... −40 to +85°C
Storage Temperature Range................................. −65 to +150°C

SWITCH TIME TEST CIRCUIT



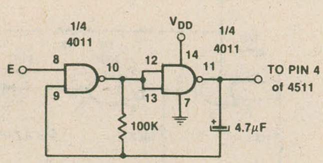
*All unused inputs of AND, NAND gates must be connected to V_{DD}.

SYNC TIMING WAVEFORMS



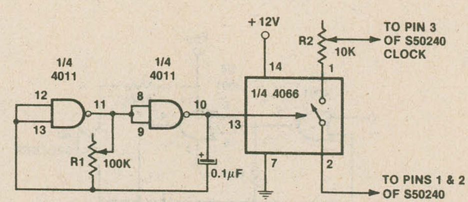
TYPICAL APPLICATIONS

E	DISPLAY
H	FLASHES
L	OFF



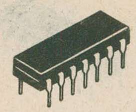
Display flashes once per second when E is high.

Display Flasher



This produces bagpipe and other unusual sounds.
Adjust R1 to vary interruption rate.

Special Effects



DUAL TYPE D FLIP-FLOP

4013
276-2413

GENERAL DESCRIPTION

The 4013 dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

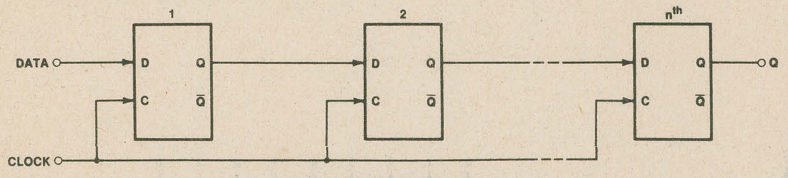
FEATURES

- Static operation
- Quiescent current = 2.0 nA/package typical @ 5 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode protection on all inputs
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Single supply operation
- Toggle rate = 4 MHz typical @ 5 Vdc
- Logic edge-clocked flip-flop design—logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.
- Capable of driving two-low-power TTL loads, one low-power schottky TTL load or two HTL loads over the rated temperature range.

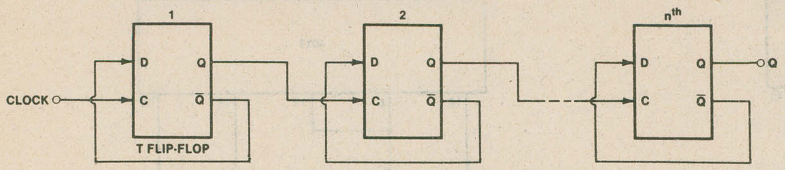
ABSOLUTE MAXIMUM RATINGS
(Voltages referenced to V_{SS})

DC Supply Voltage	−0.5 to +16 Vdc
Input Voltage, All Inputs	−0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Pin	10 mAdc
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C

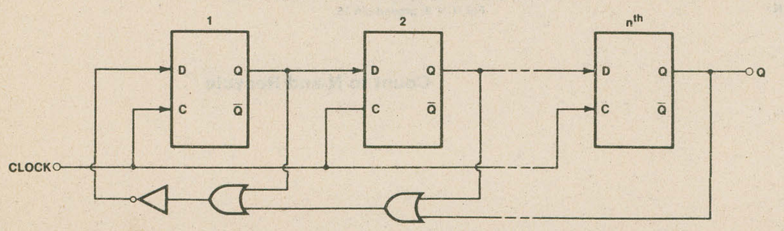
TYPICAL APPLICATIONS



n-Stage Shift Register

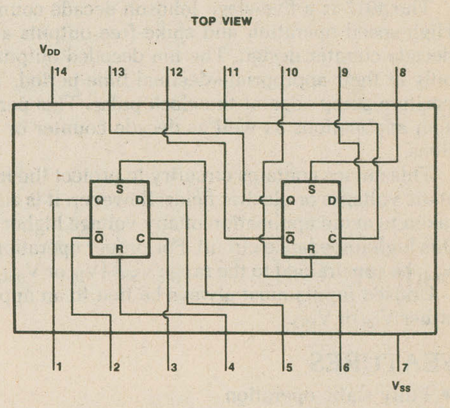


Binary Ripple Up-Counter (Divide-by-2^n)



Modified Ring Counter (Divide-by-(n+1))

PIN CONNECTION

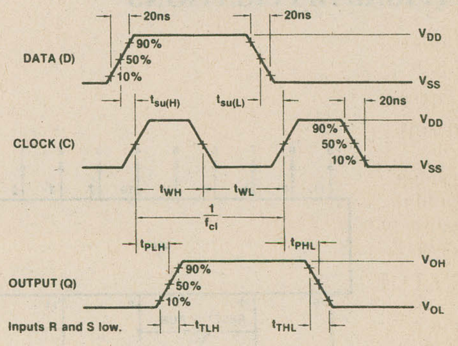


TRUTH TABLE

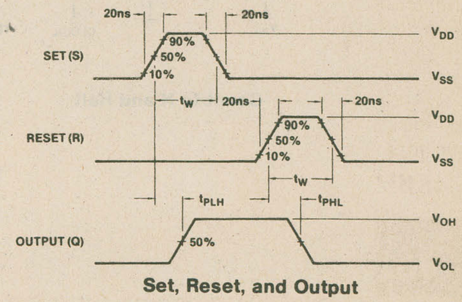
INPUTS				OUTPUTS	
Clock†	Data	Reset	Set	Q	$\overline{Q}$
_/‾	L	L	L	L	H
_/‾	H	L	L	H	L
—	X	L	L	No Change	
X	X	H	L	L	H
X	X	L	H	H	L
X	X	H	H	H	H

X = Don't Care H = High Level
L = Low Level † = Level Change

SYNC TIMING WAVEFORMS



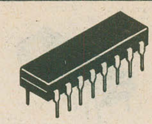
Data, Clock, and Output



Set, Reset, and Output

4017 DECADE COUNTER/DIVIDER

276-2417



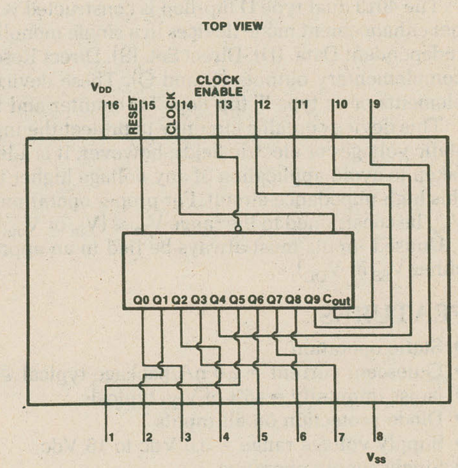
GENERAL DESCRIPTION

The 4017 is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.

PIN CONNECTION



FEATURES

- Fully static operation
- DC clock input circuit allows slow rise times
- Carry out output for cascading
- 12 MHz (typical) operation @ $V_{DD} = 10$ Vdc
- Quiescent current = 5.0 nA/package typical @ 5 Vdc
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Capable of driving two low-power TTL loads, one low-power schottky TTL load or two HTL loads over the rated temperature range

TRUTH TABLE (Positive Logic)

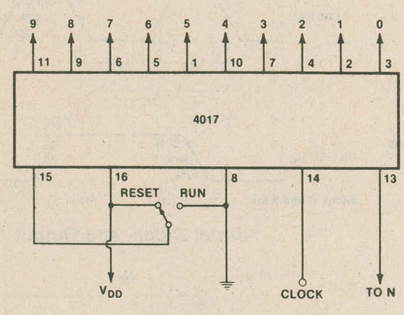
Clock	Clock Enable	Reset	Decode Output = n
L	X	L	n
X	H	L	n
X	X	H	QL
$\uparrow$	L	L	n + 1
$\downarrow$	X	L	n
X	$\uparrow$	L	n
1	$\downarrow$	L	n + 1

X = Don't Care If n <5 Carry = "H", Otherwise = "L"
L = Low Level H = High Level

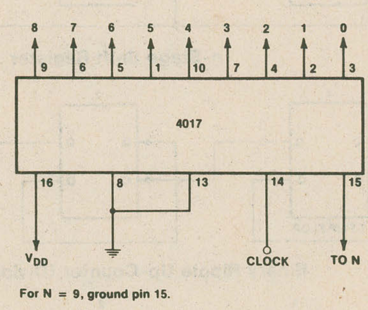
ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

DC Supply Voltage .... −0.5 to +16 Vdc
Input Voltage, All Inputs .... −0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Pin .... 10 mAdc
Operating Temperature Range .... −40 to +85°C
Storage Temperature Range .... −65 to +150°C

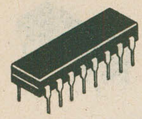
TYPICAL APPLICATIONS



Count to N and Halt



Count to N and Recycle



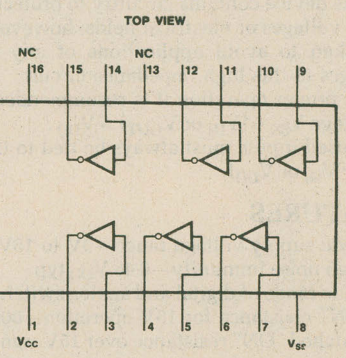
INVERTING HEX BUFFER

4049
276-2449

GENERAL DESCRIPTION

The 4049 hex inverter/buffer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC}. The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{CC} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pin 16 is not connected internally on this device; consequently connections to this terminal will not affect circuit operation.

PIN CONNECTIONS



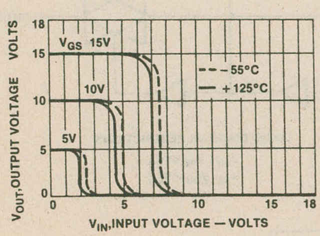
FEATURES

- High source and sink currents
- High-to-low level converter
- Quiescent current = 2.0 nA/package typical @ 5 Vdc
- Supply voltage range = 3.0 Vdc to 16 Vdc

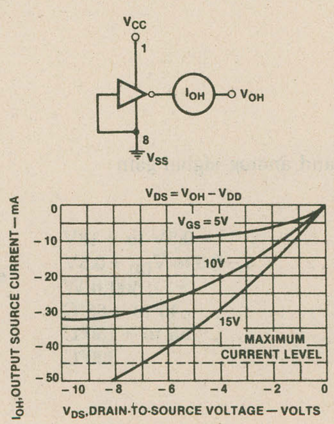
ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

DC Supply Voltage	−0.5 to +16 Vdc
Input Voltage, All Inputs	−0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Input Pin	10 mAdc
DC Current Drain per Output Pin	45 mAdc
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C

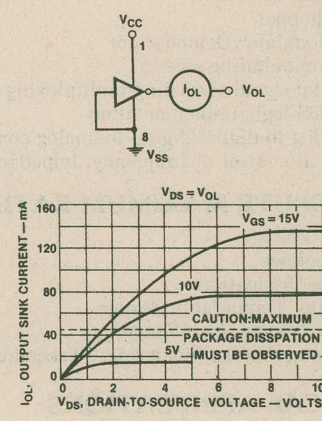
TYPICAL CHARACTERISTICS



Output Voltage vs Input Voltage

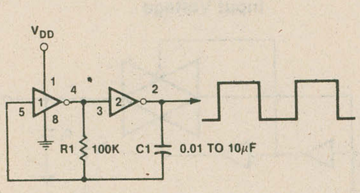


Output Source Current vs Drain-To-Source Voltage



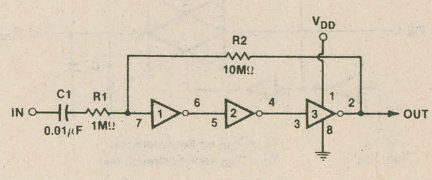
Output Sink Current vs Drain-To-Source Voltage

TYPICAL APPLICATIONS



1,2 = 1/3 4049
Pulse Rate = 1/1.4R1C1

Clock Pulse Generator

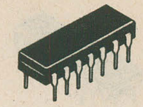


1,2,3 = 1/2 4049
Note that the inverters are used in a LINEAR mode.
Gain = R2/R1

Linear IOX Amplifier

4066 QUAD BILATERAL SWITCH

276-2466



GENERAL DESCRIPTION

The 4066 consists of four independent switches capable of controlling either digital or analog signals. This Quad Bilateral Switch is useful in signal gating, chopper, modulator, demodulator, and CMOS logic implementation.

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{DD}$.

Unused inputs must always be tied to the appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FEATURES

- Wide supply voltage range—3V to 15V
- High noise immunity—0.45 V_{DD} typ
- Wide range of digital and analog switching—±7.5 V_{PEAK}
- "ON" resistance for 15V operation—80Ω typ
- Matched "ON" resistance over 15V signal input—ΔR_{ON} = 5Ω typ
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio—65 dB typ
- High degree of linearity—<0.4% distortion typ
- Extremely low "OFF" switch leakage—0.1 nA typ
- Extremely high control input impedance—10^{12}Ω typ
- Low crosstalk between switches—−50 dB typ
- Frequency response, switch "ON"—40 MHz typ

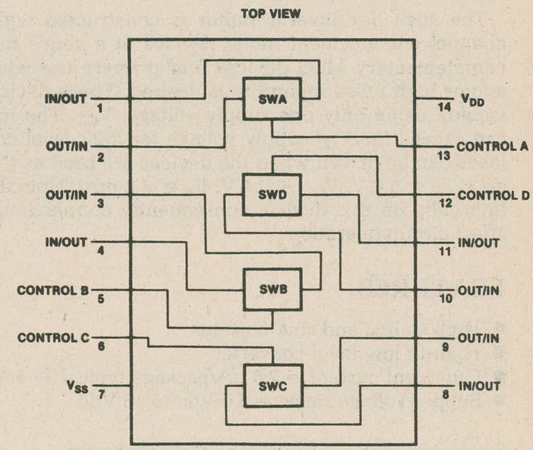
APPLICATIONS

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.5V to +18V
Input Voltage	−0.5 to V_{DD} +0.5V
Package Dissipation	500 mW
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

PIN CONNECTION

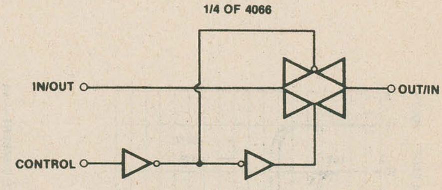


TRUTH TABLES

CONTROL	SWITCH
0	OFF
1	ON

$V_{CONTROL}$	V_{IN} TO V_{OUT} RESISTANCE
V_{SS}	$>10^9$ ohms typical
V_{DD}	3×10^2 ohms typical

LOGIC DIAGRAM

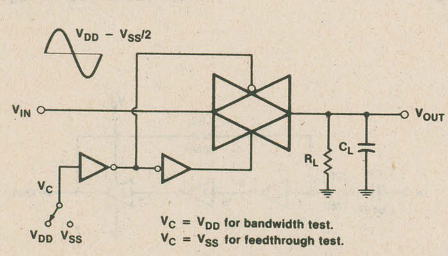


LOGIC DIAGRAM RESTRICTIONS

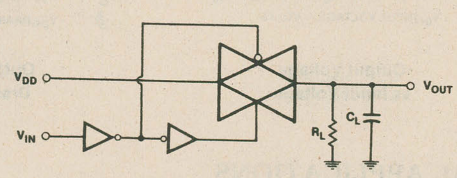
$V_{SS} < V_{IN} < V_{DD}$

$V_{SS} < V_{OUT} < V_{DD}$

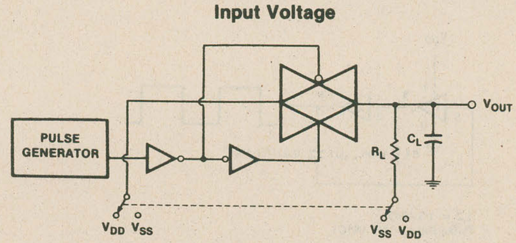
TYPICAL APPLICATIONS



Bandwidth and Feedthrough Attenuation



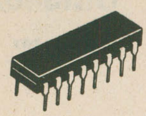
Input Voltage



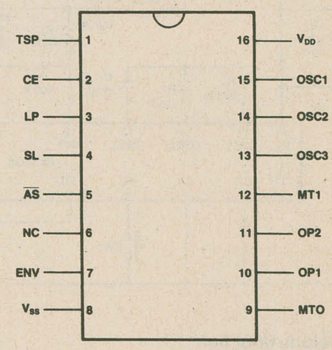
Propagation Delay Time, Control to Output

MELODY GENERATOR

UM3482
276-1797



PIN CONNECTION



GENERAL DESCRIPTION

The UM3482A is a mask-ROM-programmed multi-instrument melody generator, implemented in the CMOS technology. It is designed to play the melody according to the previously programmed information and is programmed with 12 songs with 3 instrument sounds, the piano, the organ and the mandolin. The UM3482A will play the following songs: AMERICAN PATROL, RABBITS, OH, MY DARLING CLEMENTINE, BUTTERFLY, LONDON BRIDGE IS FALLING DOWN, ROW, ROW, ROW YOUR BOAT, ARE YOU SLEEPING, HAPPY BIRTHDAY, JOY SYMPHONY, HOME SWEET HOME, WIEGENLIED, and MELODY ON PURPLE BAMBOO.

The device also includes a pre-amplifier which provides simple interface to the driver circuit.

FEATURES

- Powered by a 1.5V battery
- Low stand-by current
- 512 notes memory, up to 16 songs
- Play all the songs repeatedly or auto stop
- Play one song only, repeatedly or auto stop
- Every song starts from the first note
- Any song can be present
- 3 timbres—piano, organ and mandolin
- 5 tempos available through mask setting
- On chip envelope modulator and pre-amplifier

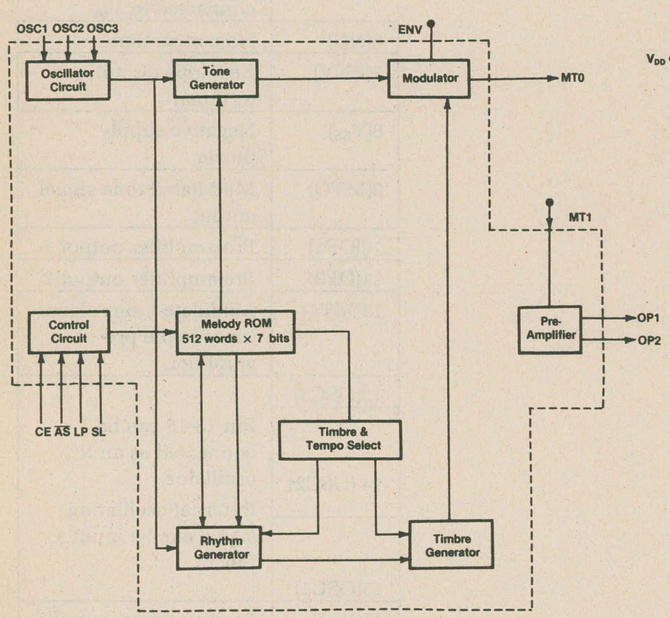
APPLICATIONS

- Toys
- Doorbells
- Music Boxes
- Melody/Clock Timers
- Telephones

ABSOLUTE MAXIMUM RATINGS

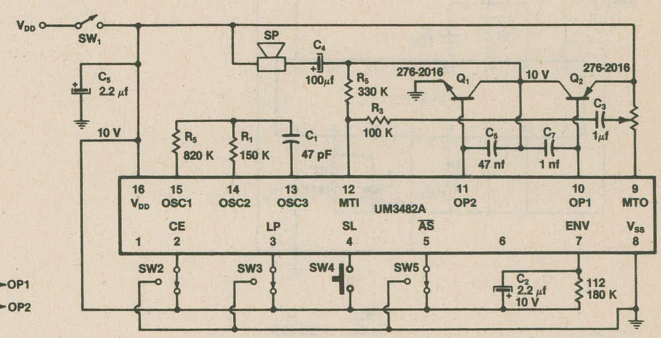
DC supply voltage .... − 0.3 V to 5.0 V
Input/output voltage .... V_{SS} − 0.3 V to V_{DD} + 0.3 V
Operating ambient temperature .... − 10°C to 60°C
Storage temperature .... − 55°C to 125°C

BLOCK DIAGRAM



TYPICAL APPLICATION

General application

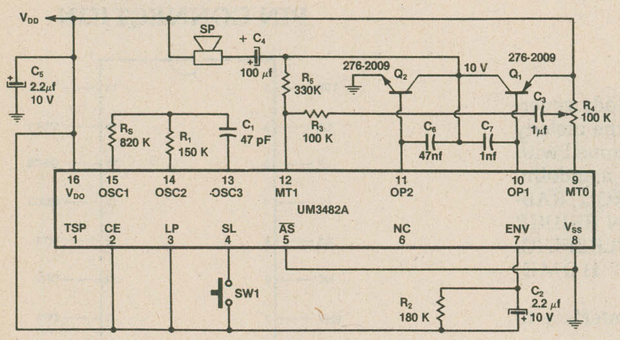


UM3482

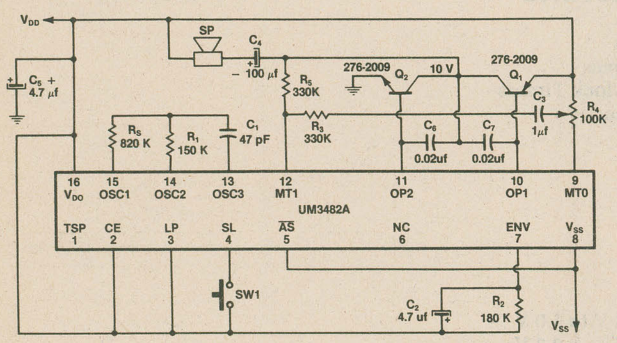
276-1797

TYPICAL APPLICATIONS

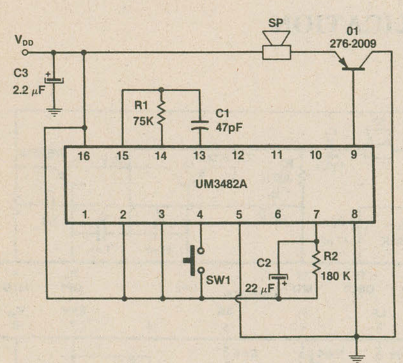
Chime function application

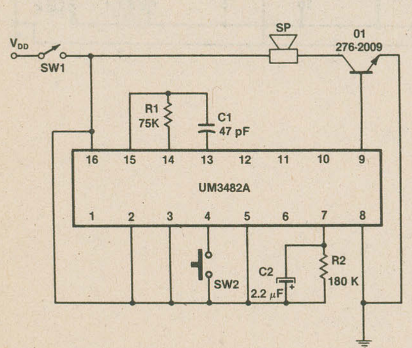


Melody door bell

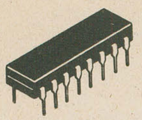


Low cost applications





PIN NAMES	FUNCTION
1(TSP)	Output flag of melody auto stop In normal operating this pin should be open
2(CE)	Chip enable if connected to V_{DD} Chip disable if connected to V_{SS}
3(LP)	The melody plays only one song if this pin connected to V_{DD} The melody plays all songs if this pin connected to V_{SS}
4(SL)	A positive going edge applied to this pin the melody will change to the next song
5($\overline{AS}$)	The melody will be repeated if this pin connected to V_{DD} The melody will be auto stop if this pin connected to V_{SS}
6(NC)	No connection
7(ENV)	Envelope circuit terminal
8(V_{SS})	Negative supply power
9(MTO)	Modulated tone signal output
10(OP1)	Pre-amplifier output 1
11(OP2)	Pre-amplifier output 2
12(MT1)	Modulated tone signal input to the pre-amplifier
13(OSC3)	Pin 13-15 can be connected as an RC oscillator External oscillating signal can be input to Pin 15
14 (OSC2)	
15(OSC1)	
16(V_{DD})	Positive power supply



65,536-BIT DYNAMIC RANDOM ACCESS MEMORY (RAM)

HYB4164-P2
276-2506

GENERAL DESCRIPTION

The HYB4164 is a 65536-word by 1-bit, MOS random access memory circuit fabricated with new 5-volt only n-channel silicon gate technology, using double layer polysilicon. To protect the chip against α-radiation a chip cover is used. The HYB4164 uses single transistor dynamic storage cells and dynamic control circuitry to achieve high speed at very low power dissipation. Multiplexed address inputs permit the HYB4164 to be packaged in an industry standard 16-pin dual-in-line package.

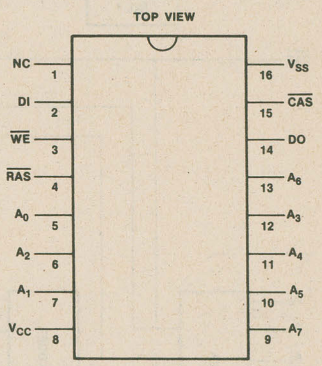
System oriented features include single power supply with ±10% tolerance, on-chip address and data latches which eliminate the need for interface registers and fully TTL compatible inputs and outputs, including clocks.

In addition to the usual read, write and read-modify-write cycles, the HYB4164 is capable of early and delayed write cycles, $\overline{RAS}$-only refresh and hidden refresh. Common I/O capability is given by using "early write" operation.

FEATURES

- 65,536 X1 bit organization
- Industry standard 16-pin JEDEC configuration
- Single +5V ±10% power supply
- Low power dissipation
  - 150 mW active (max.)
  - 20mW standby (max.)
- 150 ns access time, 280 ns cycle
- All inputs and outputs TTL compatible
- High over-and undershooting capability on all inputs
- Low supply current transients
- $\overline{CAS}$ controlled output providing latched or unlatched data
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, hidden refresh
- 256 refresh cycles with 4 ms long refresh period
- Page Mode Read and Write

PIN CONNECTION



PIN NAMES	FUNCTION
A_0 - A_7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DI	Data In
NC	No Connection
DO	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (OV)

ABSOLUTE MAXIMUM RATINGS

Voltages on any Pin relative to V_{SS} .... −1.0 to +7.0V
Voltage High Level Input (All Inputs) .... +2.4 to +6.0V
Voltage Low Level Input .... −1.0 to +0.8V
Voltage Output High (I_O = −5mA) .... +2.4 to $+V_{CC}$ V
Voltage Output Low (I_O = +4.2mA) 0.4V
Short Circuit Output Current 50mA
Power Dissipation 1.0W
Operating Temperature Range .... 0 to +70°C
Storage Temperature Range .... −65 to +150°C

FUNCTIONAL DESCRIPTIONS

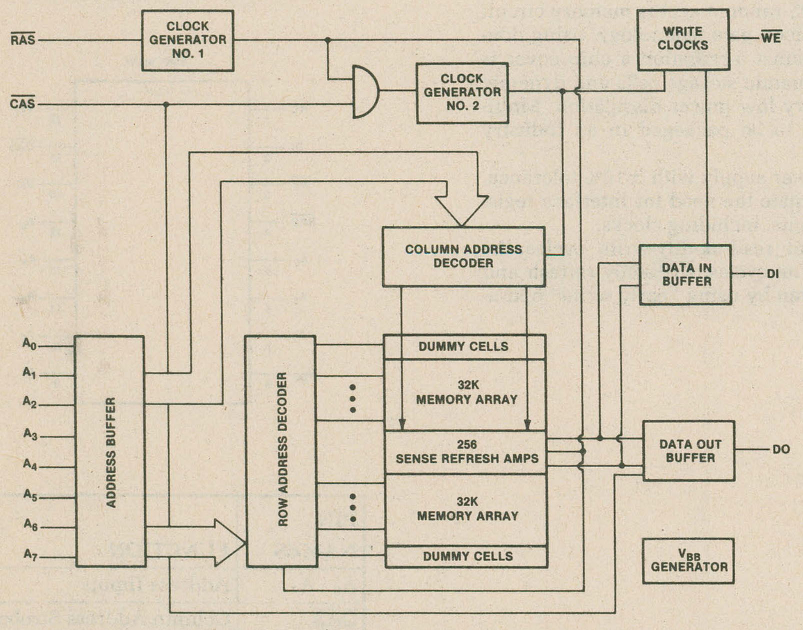
Addressing (A_0 - A_7)

For selecting one of the 65536 memory cells, a total of 16 address bits are required. First 8 row-address bits are setup on pins A_0 through A_7 and latched onto the row address latches by the Row Address Strobe ($\overline{RAS}$). Then the 8 column-address bits are set-up on pins A_0 through A_7 and latched onto the column address latches by the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or shortly after the falling edge of $\overline{RAS}$ and $\overline{CAS}$ respectively. $\overline{CAS}$ is internally gated by $\overline{RAS}$ to permit triggering of column address latches as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-address to column-address.

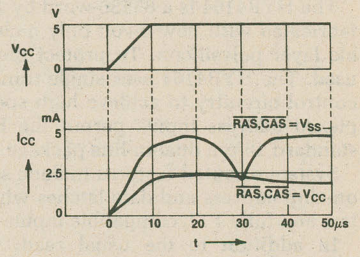
It should be noted that $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip-select activating the column decoder and the input and output buffers.

HYB4164 276-2506

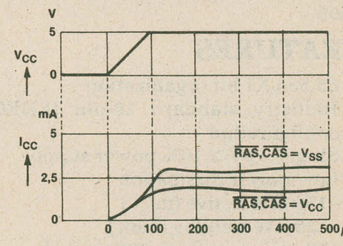
BLOCK DIAGRAM



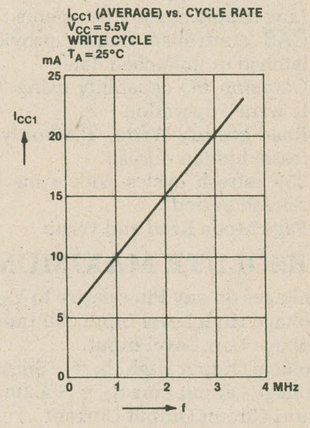
TYPICAL CHARACTERISTICS

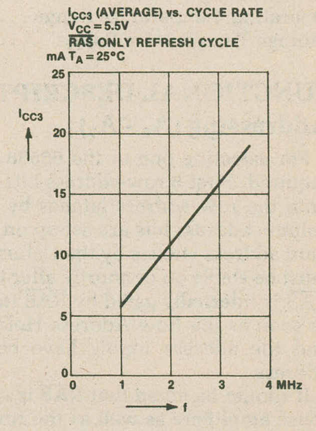


Current Consumption During Power Up (V_{CC} Risetime 10µs)



Current Consumption During Power Up (V_{CC} Risetime 100µs)





FUNCTIONAL DESCRIPTIONS (Cont'd)

Write Enable ($\overline{WE}$)

The read or write mode is selected with the $\overline{WE}$ input. A logic high (V_{IH}) on $\overline{WE}$ dictates read mode; logic low (V_{IL}) dictates write mode. The data input is disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data output (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latch. In an early write cycle $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with set-up and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with set-up and hold times referenced to this signal.

Power ON

An initial pause of 200 µs is required after power-up followed by a minimum of eight (8) initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh) prior to normal operation. The current requirement of the HYB4164 during power on is, however, dependent upon the input levels $\overline{RAS}$, $\overline{CAS}$ and the rise time of V_{CC}, as shown in the (Current Consumption During Power Up) diagram.

Data Output (DO)

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high-impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from the transition of $\overline{RAS}$ when t_{RCD} (min) is satisfied, or after t_{CAC} from the transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). $\overline{CAS}$ going high returns the output to a high-impedance state. In an early write cycle the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle.

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FUNCTIONAL DESCRIPTIONS (Cont'd)

Hidden Refresh

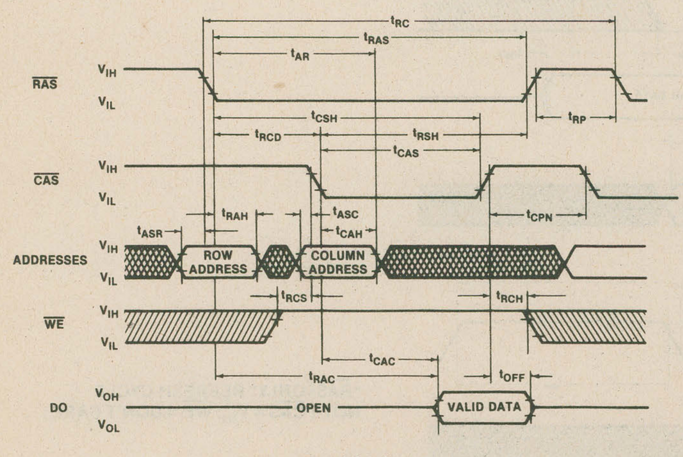
$\overline{RAS}$ only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} from a previous memory read cycle.

Page Mode

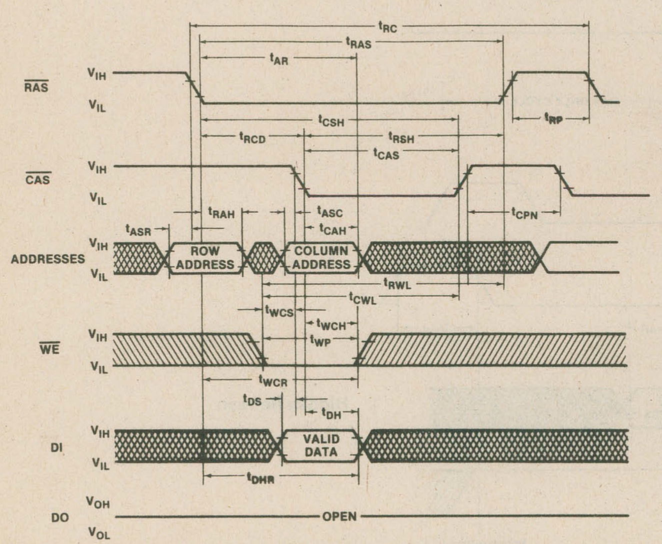
Page Mode operations allows a faster data transfer rate. This is achieved by maintaining the row address while strobing successive column addresses onto the chip. The time required to set-up and strobe sequential row addresses for the same page is eliminated.

Refresh Cycle

A refresh operation must be performed at least every four milli-seconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output signal during refresh. Strobing each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

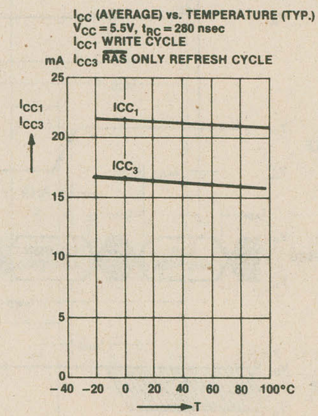


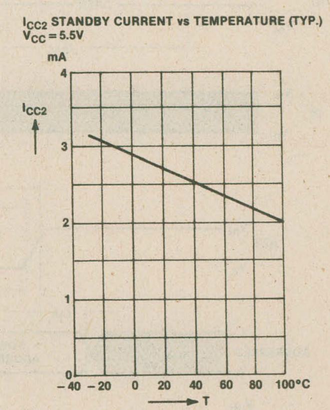
Read Cycle

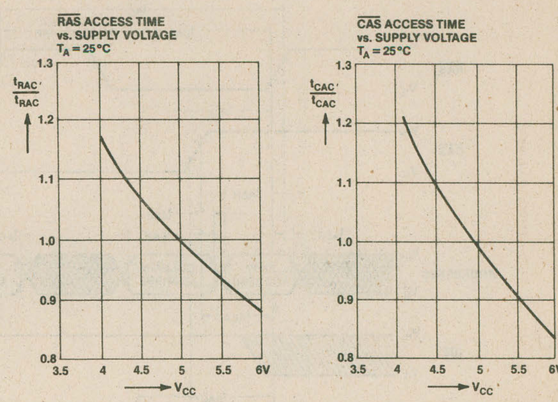


Write Cycle (Early Write)

TYPICAL CHARACTERISTICS (Cont'd)



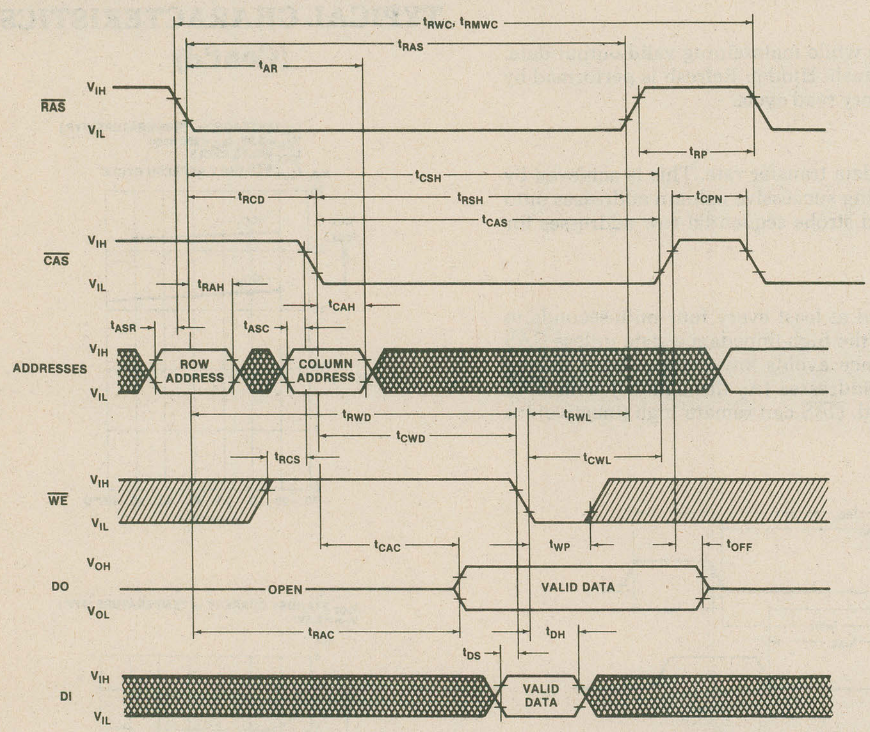




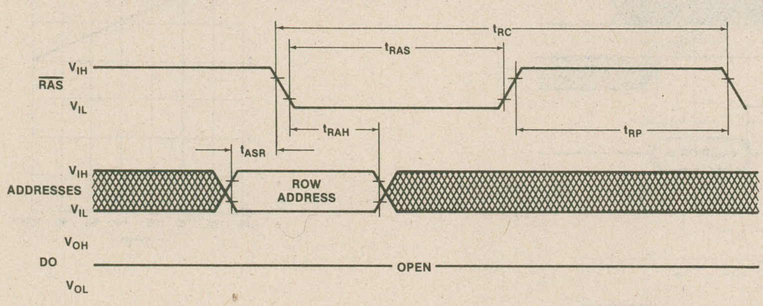
Typical Access Time Curves

HYB4164 276-2506

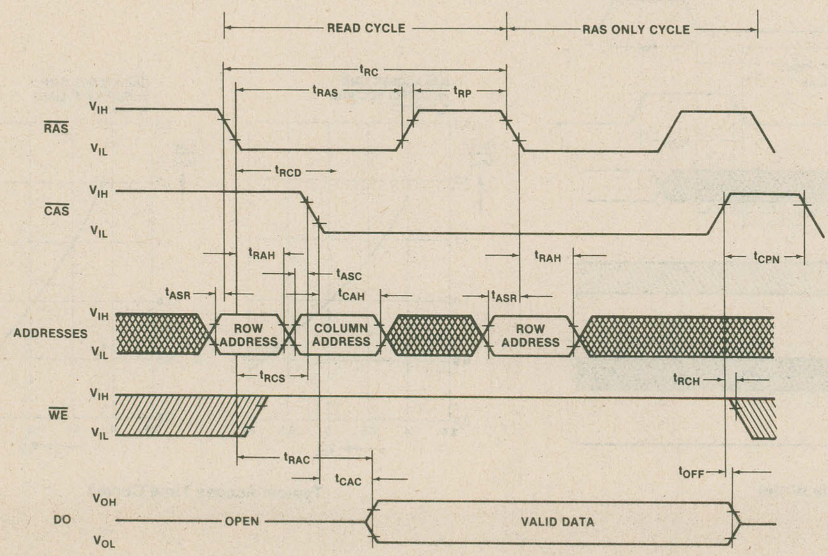
TYPICAL CHARACTERISTICS (Cont'd)



Read-Write/Read-Modify-Write Cycle



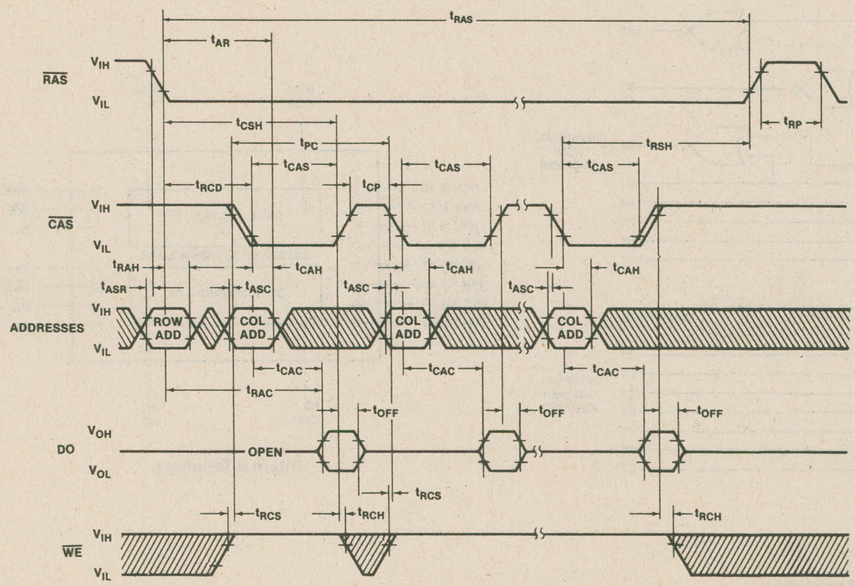
"RAS-ONLY" REFRESH CYCLE
NOTE CAS = V_{IH}; WE = DON'T CARE



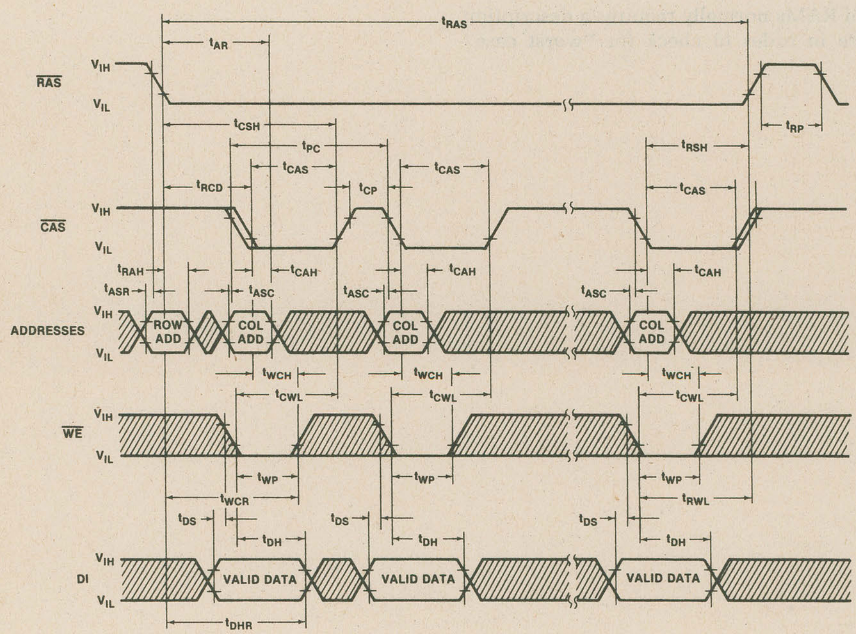
Hidden Refresh

HYB4164 276-2506

TYPICAL CHARACTERISTICS (Cont'd)



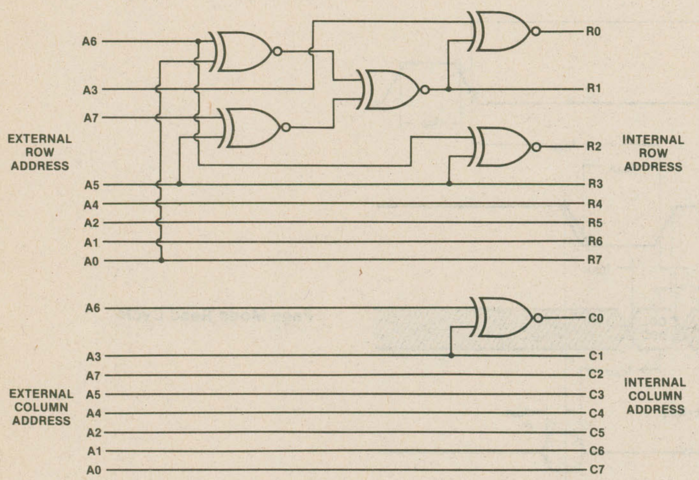
Page Mode Read Cycle



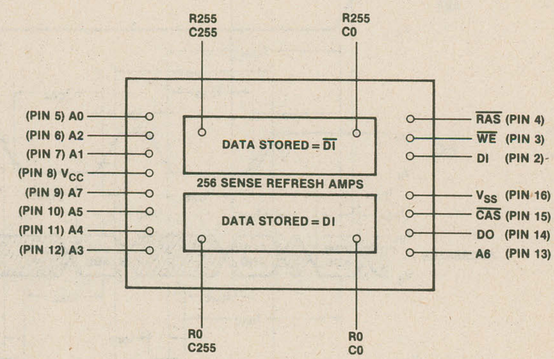
Page Mode Write Cycle

HYB4164 276-2506

TYPICAL CHARACTERISTICS (Cont'd)



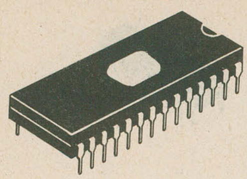
Address Decoder Scrambling



Internal Topology

Topology Description

The evaluation and incoming testing of RAMs normally requires a description of the internal topology of the device in order to check for "worst case" pattern.



64Kuv EPROM

MSM 2764RS
276-1251

GENERAL DESCRIPTION

The MSM2764RS is a 8192W × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM2764RS is ideal for microprocessor programs.

The MSM2764RS is manufactured using the N channel double silicon gate MOS technology.

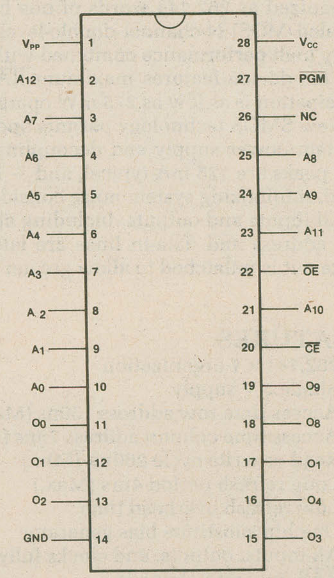
FEATURES

- +5V single power supply
- 8192 words × 8 bits configuration
- Access time: MAX 250ns
- Power consumption:
  MAX 525 mW (during operation)
  MAX 184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level (three state output)

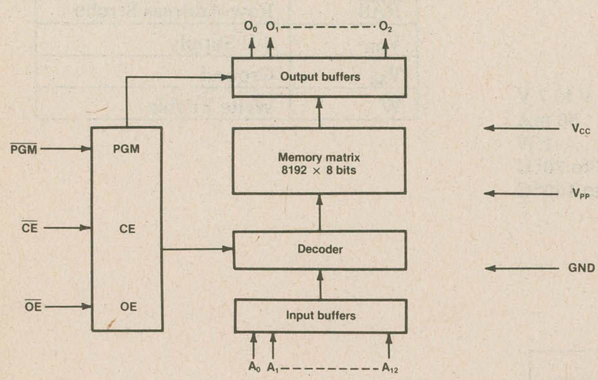
ABSOLUTE MAXIMUM RATINGS

Program Voltage V_{PP}	−0.6 V to 23 V
All input/output voltages V_{in}, V_{out}	−0.6 V to 7V
Power P_D	1.5 W
Operating Temperature T_A	0°C to 70°C
Storage Temperature $T_{S\&G}$	−55°C to 125°C

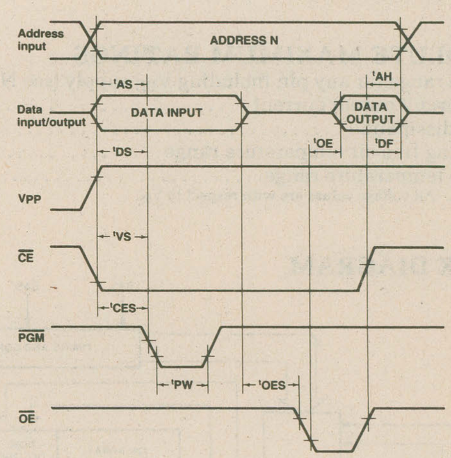
PIN CONNECTIONS



BLOCK DIAGRAM

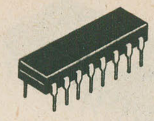


Time Chart



TMS4256
276-1252

256 K DYNAMIC RAM



GENERAL DESCRIPTION

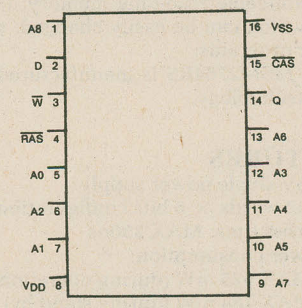
The 4256 is a high-speed, 262,144-bit dynamic random-access memory, organized as 262,144 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

This device features maximum $\overline{RAS}$ access times of 150ns. Typical power dissipation is as low as 275 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 125 mA typical, and −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

PIN CONNECTION



FEATURES

- 262,144 × 1 organization
- Single 5 V supply
- Access time row address 150ns (Max.)
- Access time column address 75ns (Max.)
- Read or write cycle 260ns (Min.)
- Long refresh period 4ms (Max.)
- Low refresh overhead time
- On-chip substitute bias generator
- All inputs, outputs, and clocks fully TTL compatible
- $\overline{RAS}$-only refresh mode
- Hidden refresh mode
- $\overline{CAS}$-before-$\overline{RAS}$ refresh mode

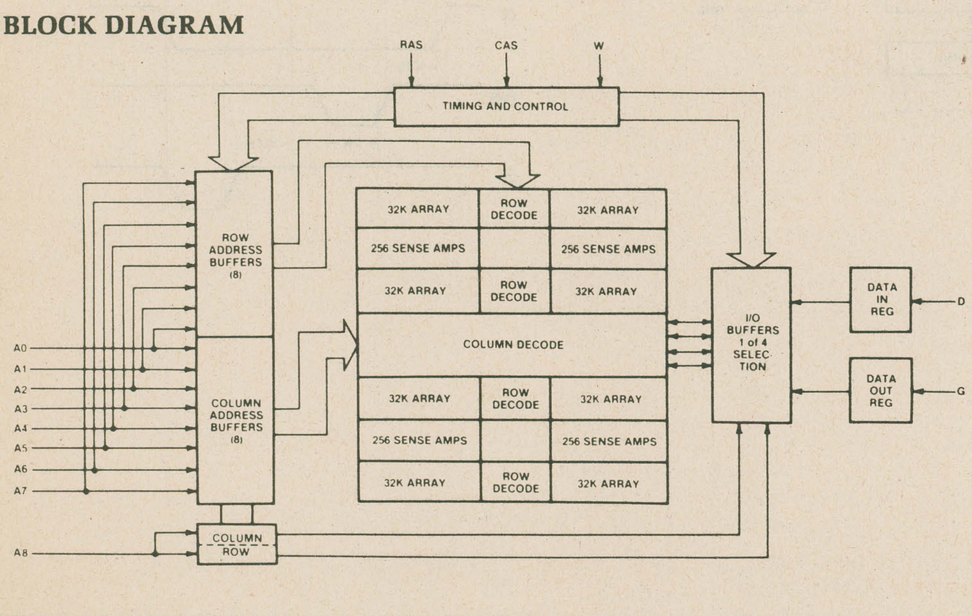
TRUTH TABLE

PIN NAMES	FUNCTION
A0–A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

ABSOLUTE MAXIMUM RATINGS

Voltage range for any pin including V_{DD} supply (see Note 1) ...... −1 V to 7 V
Short circuit output current .... 50 mA
Power dissipation .... 1 W
Operating free-air temperature range .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
NOTES: 1. All voltage values are with respect to V_{SS}.

BLOCK DIAGRAM



OPERATION

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{\text{RAS}}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{\text{CAS}}$). All addresses must be stable on or before the falling edges of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. $\overline{\text{RAS}}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{\text{CAS}}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{\text{W}}$)

The read or write mode is selected through the write-enable ($\overline{\text{W}}$) input. A logic high on the $\overline{\text{W}}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{\text{W}}$ goes low prior to $\overline{\text{CAS}}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{W}}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{\text{W}}$ is brought low prior to $\overline{\text{CAS}}$ and the data is strobed in by $\overline{\text{CAS}}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{\text{CAS}}$ will already be low, thus the data will be strobed in by $\overline{\text{W}}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{\text{CAS}}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{\text{CAS}}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{\text{CAS}}$ is low; $\overline{\text{CAS}}$ going high returns it to a high-impedance state. In a read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0–A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is utilized by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CRL}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CLRL}). For successive $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{CAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a "$\overline{\text{RAS}}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page mode

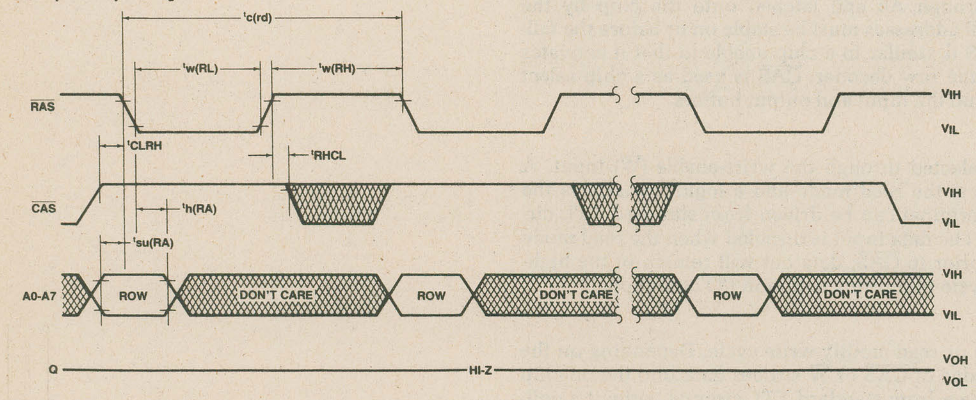
Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{w(RL)}$, the maximum $\overline{\text{RAS}}$ low pulse duration.

power-up

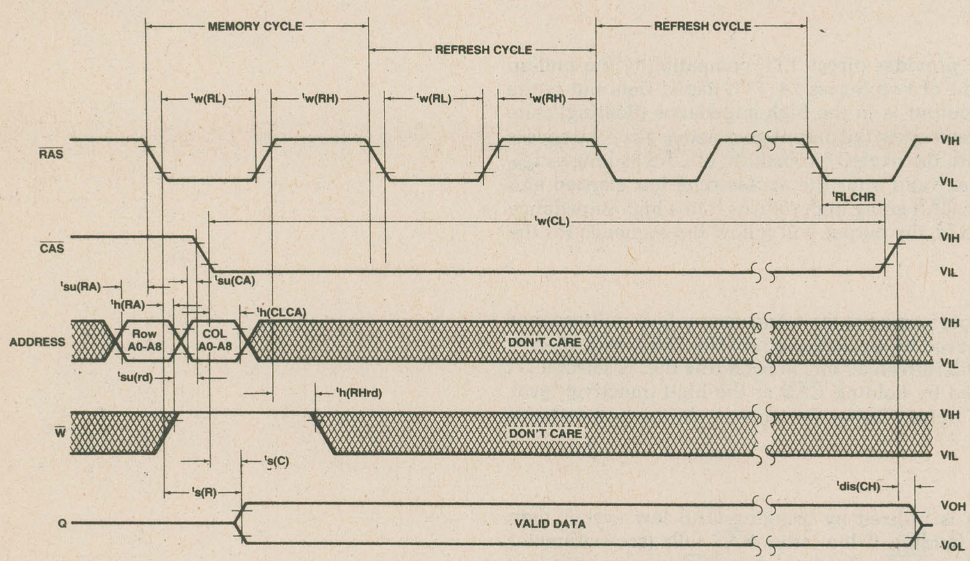
To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

TMS 4256 276-1252

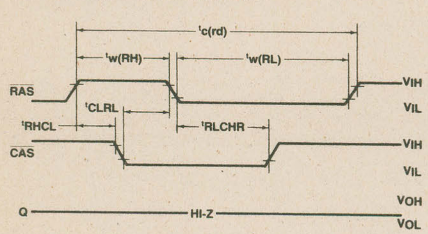
$\overline{RAS}$-only refresh cycle timing

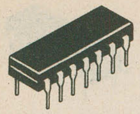


hidden refresh cycle timing



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing





QUAD TWO-INPUT NAND GATE

7400
276-1801

GENERAL DESCRIPTION

This device employs TTL logic to achieve high speed at moderate power dissipiation. It provides the basic functions used in the implementation of digital integrated circuit systems.

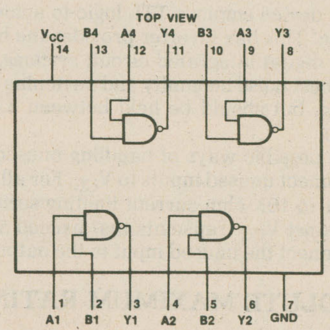
For best noise immunity and switching speed, unused inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways at handling unused inputs are:

(1) Connect unused inputs to V_{CC}. For all multi-emitter conventional TTL inputs, A 1 to 10K ohm current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

(2) Connect the unused input to the output of an unused gate that is forced high.

PIN CONNECTION



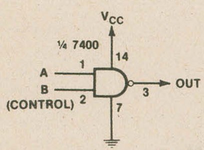
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} .... 5.25 V
Input High Voltage .... 2.0 V
Input Low Voltage .... 0.8 V
Input Clamp Diode Voltage (V_{CC} = 5.0 V, I_{IN} = − 12 mA) .... − 1.5 V
Input High CUrrent (V_{CC} = Max., V_{IN} = 2.4 V) .... 40 μA
Input Low Current (V_{CC} = Max., V_{IN} = 0.4 V) .... − 1.6 mA
Operating Temperature .... 0 to + 70°C

TRUTH TABLE

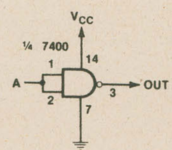
$Y=\overline{AB}$

TYPICAL APPLICATIONS



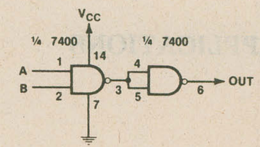
A	B	OUT
L	L	H
L	H	H
H	L	H
H	H	L

Control Gate



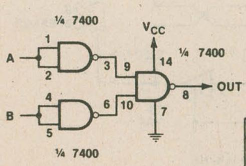
A	OUT
L	H
H	L

Inverter



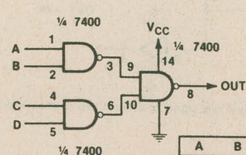
A	B	OUT
L	L	L
L	H	L
H	L	L
H	H	H

AND Gate



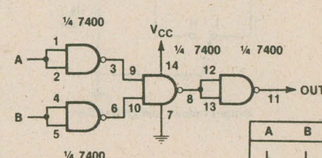
A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	H

OR Gate



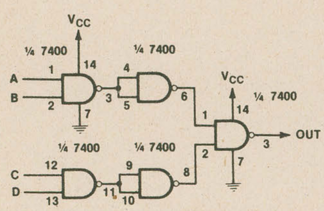
A	B	C	D	OUT
X	X	H	H	H
H	H	X	X	H
H	H	H	H	H

AND-OR Gate



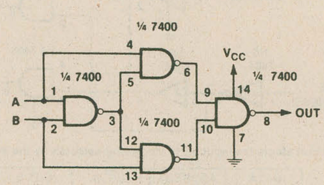
A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

NOR Gate



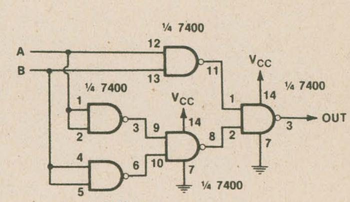
A	B	C	D	OUT
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

4-Input NAND Gate



A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	L

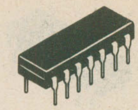
Exclusive-OR Gate



A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	H

Exclusive-NOR Gate

7404 HEX INVERTER
276-1802



GENERAL DESCRIPTION

This device employs TTL logic to achieve high speed at moderate power dissipation. This hex inverter provides the basic functions used in the implementation of digital integrated circuit systems.

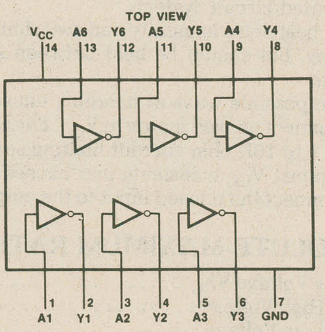
For best noise immunity and switching speed, unused inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

(1) Connect unused inputs to V_{CC}. For all multi-emitter conventional TTL inputs, A 1 to 10K ohm current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

(2) Connect the unused input to the output of an unused gate that is forced high.

PIN CONNECTION



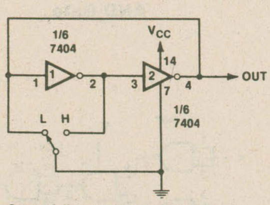
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} .... 5.25 V
Input High Voltage .... 2.0 V
Input Low Voltage .... 0.8 V
Input Clamp Diode Voltage (V_{CC} = 5.0 V, I_{IN} = − 12 mA) .... − 1.5 V
Input High Current (V_{CC} = Max., V_{IN} = 2.4 V) .... 40 μA
Input Low Current (V_{CC} = Max., V_{IN} = 0.4 V) .... − 1.6 mA
Operating Temperature .... 0 to + 70°C

TRUTH TABLE

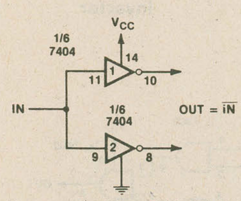
$Y = \overline{A}$

TYPICAL APPLICATIONS



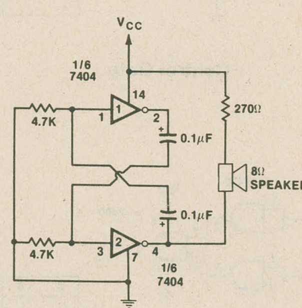
Output follows switch position.

Bouncefree Switch



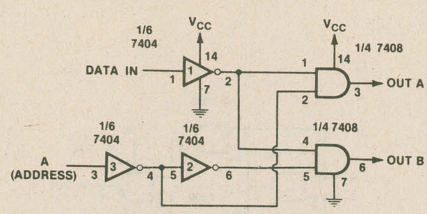
Allows one signal to control two or more inputs.

Universal Expander



Output tone is 4kHz.

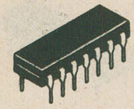
Audio Oscillator



This circuit steers the input bit to the output selected by the address.

DATA	ADDRESS	OUT A	OUT B
L	L	L	H
H	L	H	H
L	H	H	L
H	H	H	H

1-of-2 Demultiplexer



QUAD TWO-INPUT AND GATE

7408
276-1822

GENERAL DESCRIPTION

This device employs TTL logic to achieve high speed at moderate power dissipation. These gates provide the basic functions used in the implementation of digital integrated circuit systems.

For best noise immunity and switching speed, unused inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways at handling unused inputs are:

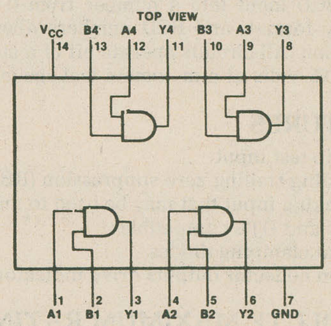
(1) Connect unused inputs to V_{CC}. For all multi-emitter conventional TTL inputs, a 1 to 10K ohm current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

(2) Connect the unused input to the output of an unused gate that is forced high.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} .... 5.25 V
Input High Voltage .... 2.0 V
Input Low Voltage .... 0.8 V
Input Clamp Diode Voltage (V_{CC} = 5.0 V, I_{IN} = − 12 mA) .... − 1.5 V
Input High Current (V_{CC} = Max., V_{IN} = 2.4 V) .... 40 μA
Input Low Current (V_{CC} = Max., V_{IN} = 0.4 V) .... − 1.6 mA
Operating Temperature .... 0 to + 70°C

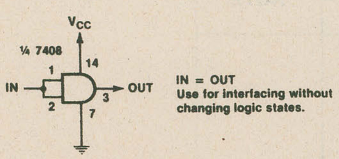
PIN CONNECTION



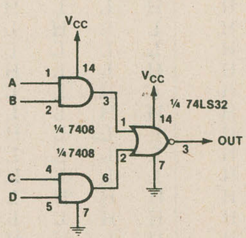
TRUTH TABLE

Y=AB

TYPICAL APPLICATIONS

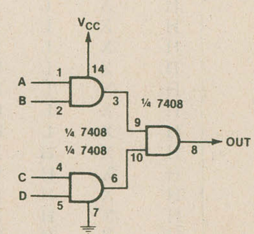


AND Gate Buffer



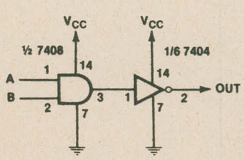
A	B	C	D	OUT
X	X	X	X	H
L	L	X	X	L
L	L	L	L	L

AND-OR-Invert Gate



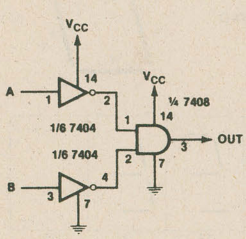
A	B	C	D	OUT
H	H	H	H	H
X	X	X	X	L

4-Input AND Gate



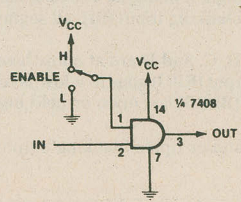
A	B	OUT
L	L	H
L	H	H
H	L	H
H	H	L

NAND Gate



A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

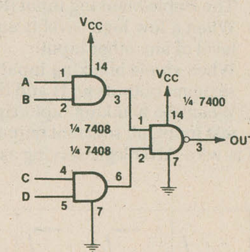
NOR Gate



IN	E	OUT
L	L	L
L	H	L
H	L	L
H	H	H

E = ENABLE

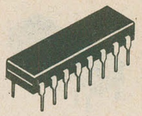
Digital Transmission Gate



A	B	C	D	OUT
H	H	H	H	L
X	X	X	X	H

4-Input NAND Gate

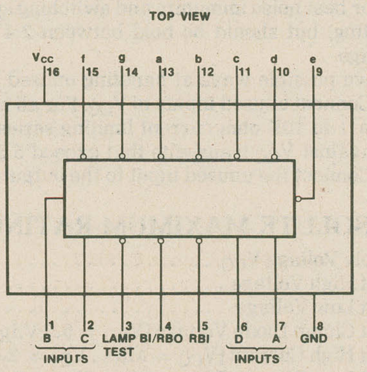
7447 276-1805 BCD TO SEVEN-SEGMENT DECODER/DRIVER



GENERAL DESCRIPTION

This versatile binary-coded-decimal 7-segment display driver fulfills a wide variety of requirements for most active high (common cathode) and active low (common anode) light emitting diodes (LED) or lamp displays. It fully decodes a 4-bit BCD input into a number from 0 through 9 in the standard 7-segment display format, and BCD numbers above 9 into unique patterns that verify operation. All circuits operate off of a single 5.0V supply. The output will withstand 15 Volts at a maximum leakage current of 250μA.

PIN CONNECTION



FEATURES

- Lamp-test input
- Leading trailing zero suppression (RBI and RBO)
- Blanking input that may be used to modulate lamp intensity or inhibit output
- TTL and DTL compatible
- Input clamping diodes
- Open collector outputs drive indicators directly

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} .... 4.75 — 5.25 V
Continuous Voltage at Outputs a-g .... Max. 15 V
Logic 1 Input Voltage .... Min. 2 V
Logic 0 Input Voltage .... Max. 0.8 V
Logic 0 Output Voltage BI/RBO .... Max. 0.4 V
Logic 1 Output Voltage at BI/RBO .... Min. 2.4 V
Power .... 320 mW

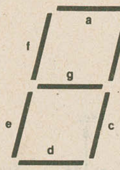
TRUTH TABLE

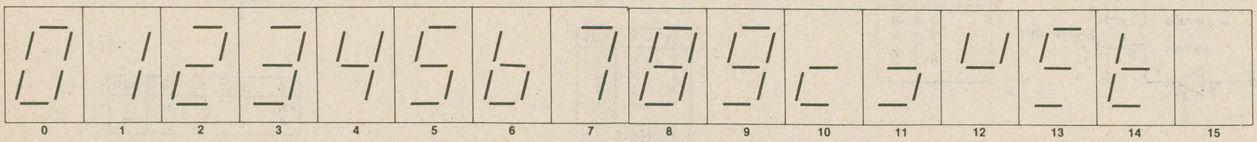
DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	1
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	2
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	3
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	4

H = High Level, L = Low Level, X = Irrelevant

Notes:
1. The blanking input (BI) must be open or held at a high logic level when output functions 0 thru 15 are desired. The ripple-blanking input (RBI) must be open or high, if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are H regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp test input, all segment outputs are L.

† BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

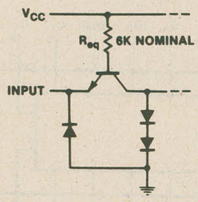




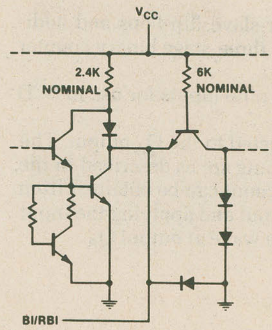
Numerical Designations and Resultant Displays

7447 276-1805

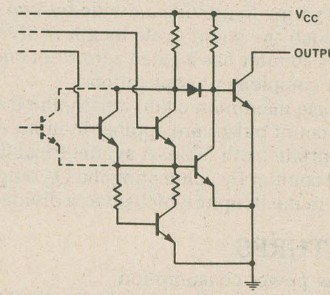
INPUT/OUTPUT EQUIVALENTS



Each Input Except BI/RBO

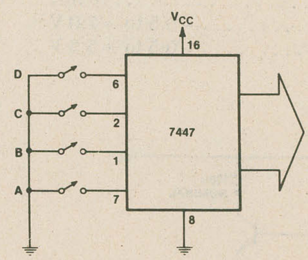


BI/RBO Input

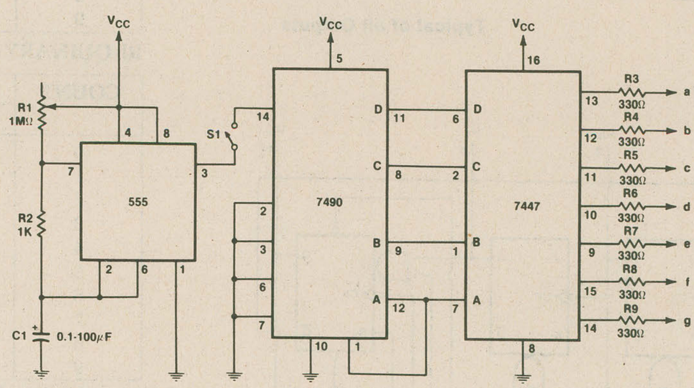


Typical of Outputs a Thru g

TYPICAL APPLICATIONS



Manually Switched Display

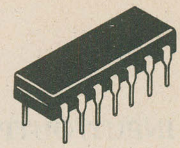


Close S1 to start timing cycle.
Calibrate 555 for 1 pulse (count) per second or 1 count per minute by adjusting R1.

0-9 Second/Minute Timer

7490
276-1808

DIVIDE BY 2 OR 5, BCD COUNTER



GENERAL DESCRIPTION

This monolithic BCD counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

This counter has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

To use maximum count length, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

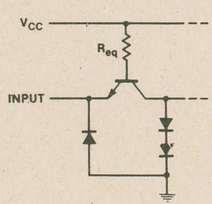
FEATURES

- Low power consumption
- High count rates . . . typically 50MHz
- Choice of counting modes
- Fully TTL and CMOS compatible

ABSOLUTE MAXIMUM RATINGS

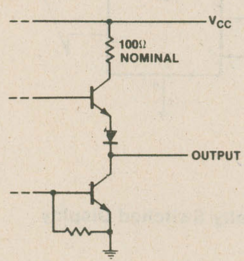
Typical Power Dissipation	145 mW
Count Frequency	42 MHz
High Level Input Voltage (Min)	2 V
Low Level Input Voltage (Max)	0.8 V
High Level Input Current	800 μA
Low Level Output Current (Max)	16 mA
V_{CC} to Ground	– 0.5 to + 7.0 V
Voltage Applied to Outputs (Output High)	– 0.5 to + 5.5 V

INPUT/OUTPUT EQUIVALENTS



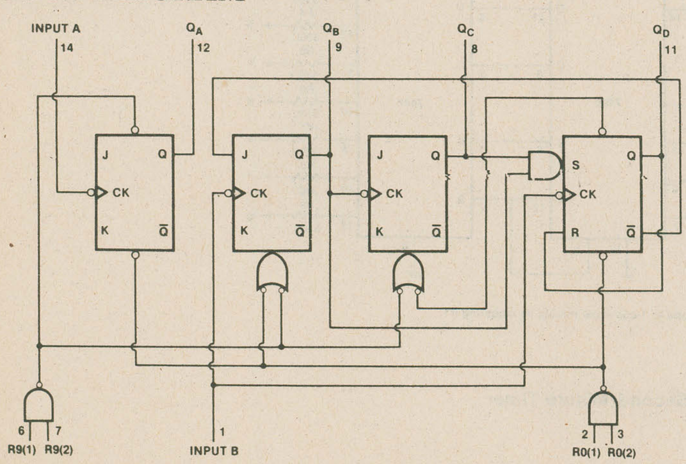
INPUT	R_{eq} NOMINAL
A	2.5K
B	1.25K
ALL RESETS	6K

Each Input



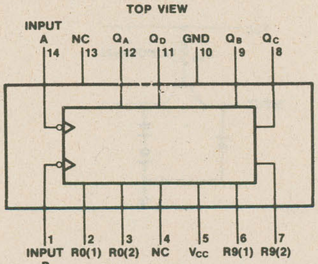
Typical of all Outputs

BLOCK DIAGRAM



PIN CONNECTION

TOP VIEW



TRUTH TABLES

RESET/COUNT

RESET INPUTS				OUTPUTS			
RO(1)	RO(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

BCD COUNT SEQUENCE (See Note A)

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (See Note B)

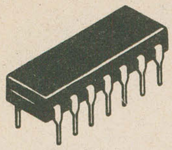
COUNT	OUTPUTS			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

L = Low Level
H = High Level

Notes:

(A) Output Q_A is connected to input B for BCD count.

(B) Output Q_D is connected to input A for bi-quinary count.



QUAD LINE DRIVER

MC1488
276-2520

GENERAL DESCRIPTION

The 1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

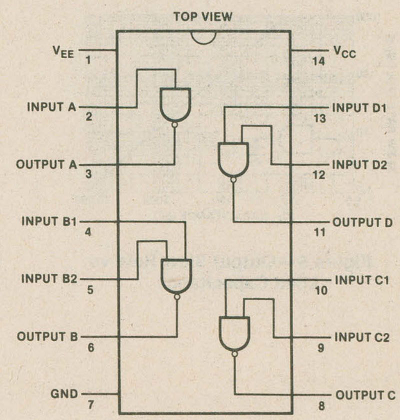
FEATURES

- Current Limited Output
  ±10 MA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range

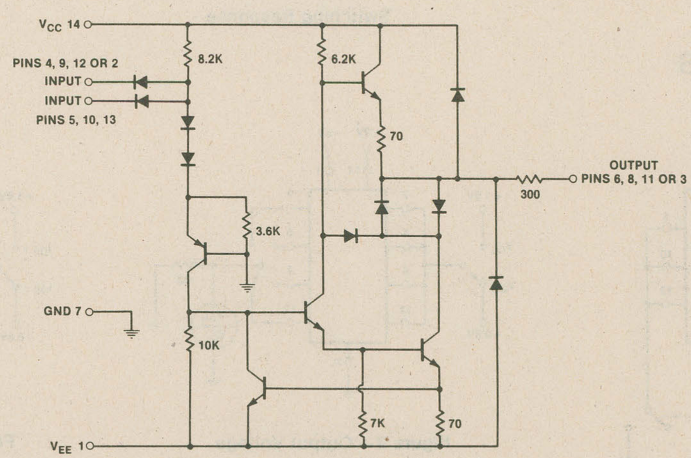
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	15 V
(V_{EE})	− 15 V
Output Signal Voltage (VO)	±15 V
Power (PD)	1 W
Input Current-Low Logic State (V_{IL} = 0) (See Fig. 8)	1.6 mA
Input Current-High Logic State (V_{IH} = 5.0V) (See Fig. 8)	10 μA
Output Resistance (V_{CC} = V_{EE} = 0/Vol = ±2.0V (See Fig. 11)	300Ω
Operating Temperature Range (TA)	0°C To + 75°C
Storage Temperature Range (T_{stg})	−65°C To +175°C

PIN CONNECTION



INTERNAL CIRCUIT (¼ of Circuit Shown)



TYPICAL CHARACTERISTICS

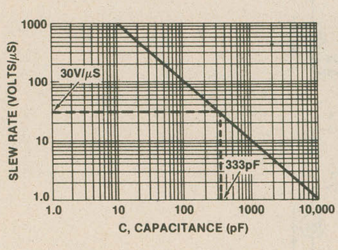


Figure 1—Slew Rate vs Capacitance for I_{SC} = 10mA

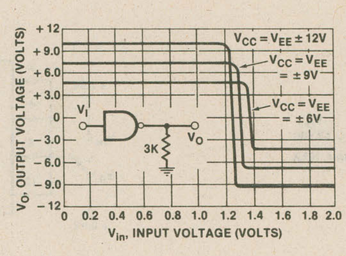


Figure 3—Transfer Characteristics vs Power-Supply Voltage

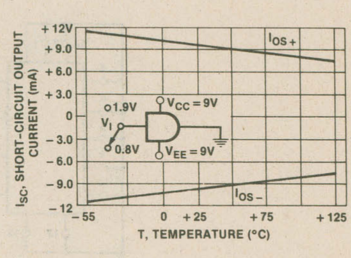


Figure 4—Short-Circuit Output Current vs Temperature

MC1488 276-2520

TYPICAL CHARACTERISTICS (Cont'd)

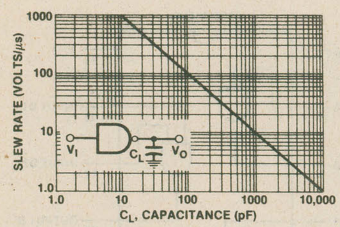


Figure 5—Output Slew Rate vs Load Capacitance

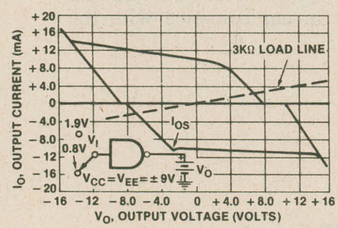


Figure 6—Output Voltage and Current-Limiting Characteristics

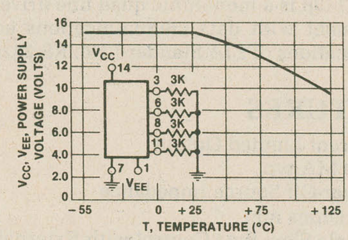
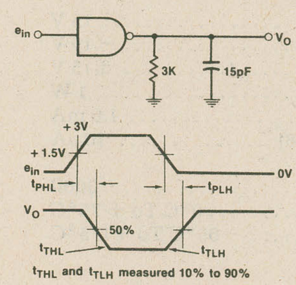


Figure 7—Maximum Operating Temperature vs Power-Supply Voltage



Switching Response

TEST CIRCUITS

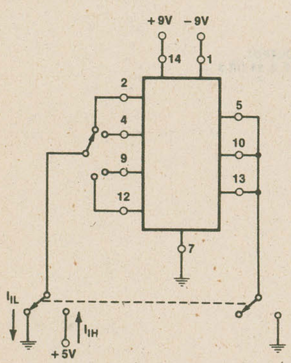


Figure 8— Input Current

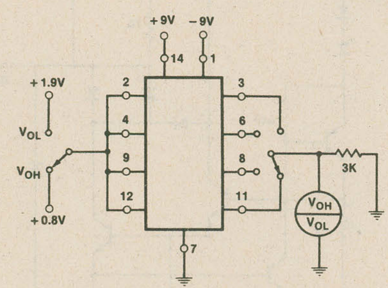


Figure 9— Output Voltage

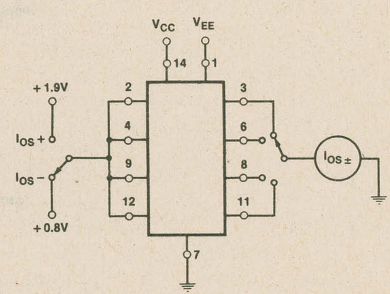


Figure 10— Output Short-Circuit Current

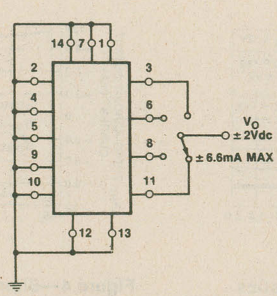


Figure 11— Output Resistance (Power-Off)

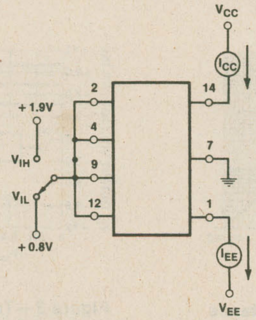


Figure 12— Power-Supply Currents

APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) RS232C specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The 1488 quad driver and its companion circuit, the 1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "O" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The 1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the 1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each drive output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 1 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The 1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geq 9.0$ V; $V_{EE} \leq -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the 1488 effectively shorting the 300-ohm output resistors to ground. If *all four outputs* were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 2, could be used to decouple all the driver packages in a system. (These same diodes will allow the 1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the 1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

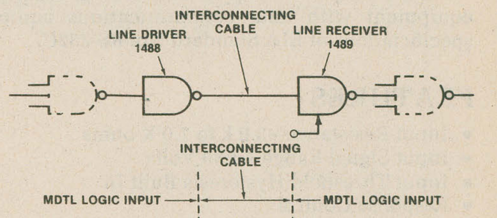
The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

OTHER APPLICATIONS

The 1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting—this enables the circuit designer to define the output voltage levels independing of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the 1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.
2. Power-Supply Range—as can be seen from the schematic drawing of the drivers, the postive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately −2.5 volts to the minimum specified −15 volts. The 1488 will drive the output to within 2 volts of the postive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL or DTL translation. Figure 15 shows one such combination.

TYPICAL APPLICATIONS



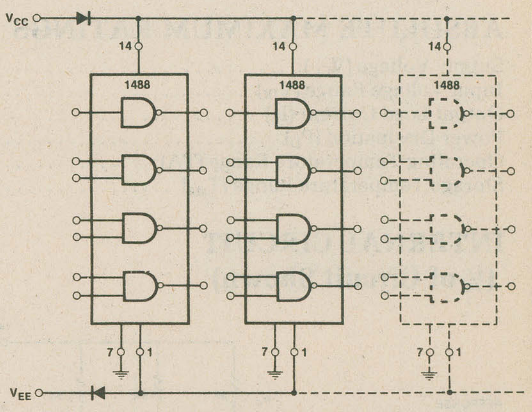


Figure 2—Power Supply Protection to Meet Power-Off Fault Conditions

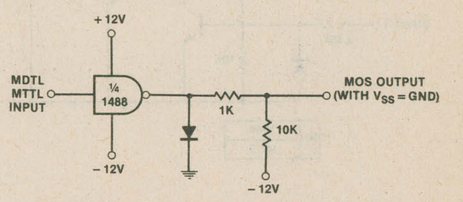


Figure 14—MDTL/MTTL-to-MOS Translator

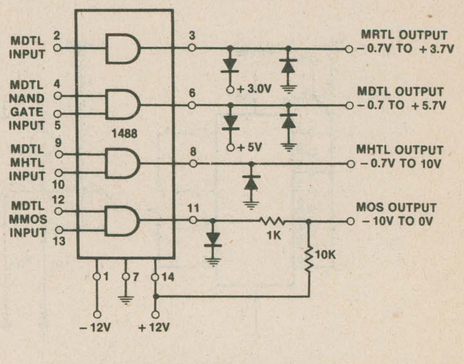
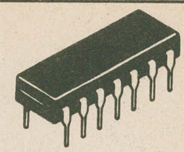


Figure 15—Logic Translator Applications

MC1489 QUAD LINE RECEIVER

276-2521



GENERAL DESCRIPTION

The 1489 monolithic quad line receiver is designed to interface data terminal equipment with data communications equipment in conformance with specificiations of EIA Standard No. RS-232C.

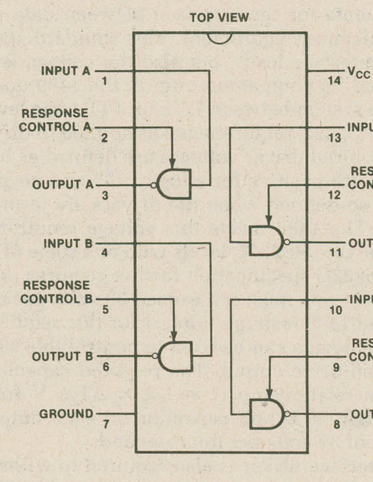
FEATURES

- Input Resistance—3.0 k to 7.0 K ohms
- Input Signal Range—±30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

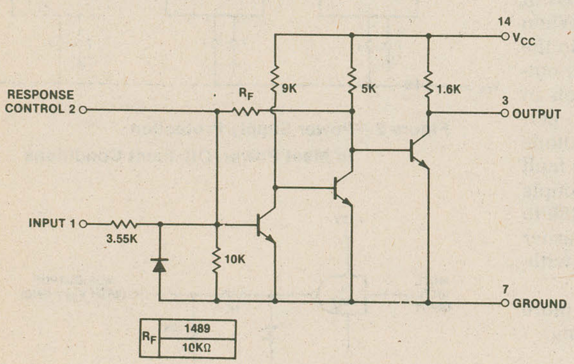
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	10 V
Input Voltage Range (V_{IR})	±30 V
Output Load Current (I_L)	20 mA
Power Dissipation (P_D)	1 W
Operating Temperature Range (TA)	0°C To +75°C
Storage Temperature Range (T_{stg})	−65°C To +175°C

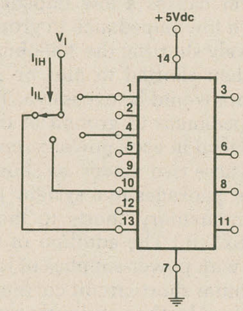
PIN CONNECTION



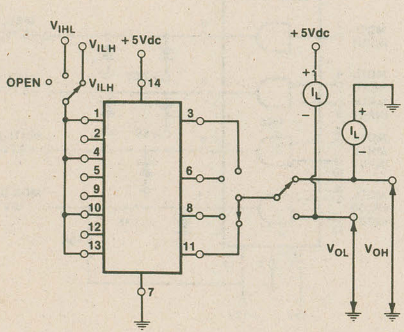
INTERNAL CIRCUIT (¼ of Circuit Shown)



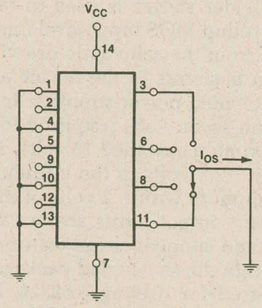
TEST CIRCUITS



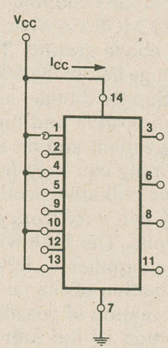
Input Current



Output Voltage and Input Threshold Voltage



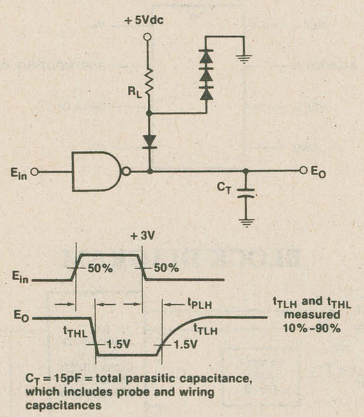
Output Short-Circuit Current



Power-Supply Current

MC1489 276-2521

TYPICAL CHARACTERISTICS



Switching Response

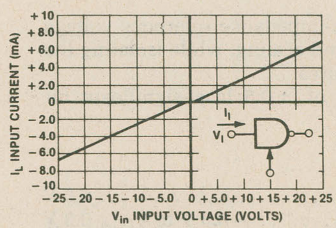


Figure 1—Input Current

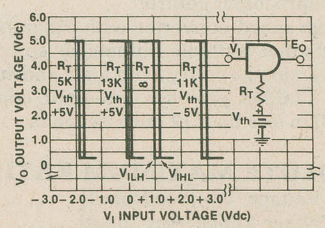


Figure 2—Input Threshold Voltage Adjustment

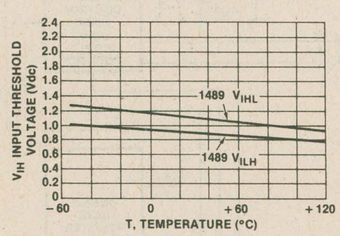


Figure 3—Input Threshold Voltage vs Temperature

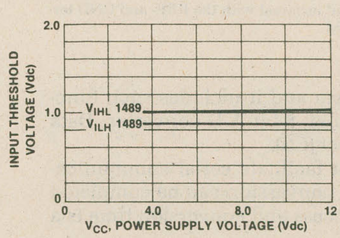


Figure 4—Input Threshold vs Power—Supply Voltage

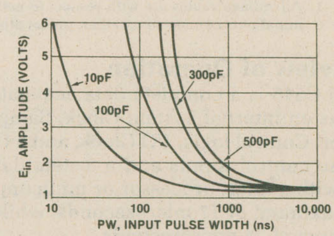


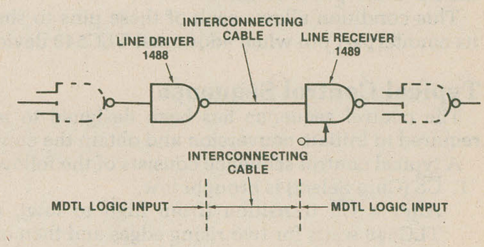
Figure 5—Turn-on Threshold vs Capacitance from Response Control Pin to Gnd

APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The 1488 quad driver and its companion circuit, the 1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed here. The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The 1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between −3.0 and −25 volts as a logic "1" and input between +3.0 and +25 volts as a logic "0". On some interchange leads, an open circuit or power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or logic "1". For this reason, the input hysteresis thresholds of the 1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative of logic "1" input.

TYPICAL APPLICATIONS



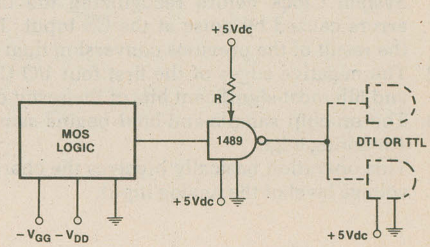
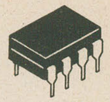


Figure 7—Typical Translator Application—MOS to DTL or TTL

TLC548
276-1796

LINCMOS 8-BIT ANALOG TO DIGITAL CONVERTER



GENERAL DESCRIPTION

The TLC548 8-bit Analog-to-Digital Converter is a complete data acquisition system on a single chip. It is designed for serial interface with a microprocessor, peripheral, or digital logic circuitry through 3-state Data Output, Chip Select, and I/O Clock control signals.

FEATURES

- Versatile control logic
- An on-chip sample-and-hold circuit that can operate automatically or under microprocessor control
- A high-speed converter with differential high-impedance reference voltage inputs that facilitate ratiometric conversion and scaling, while isolating the conversion circuitry from logic and supply noises.
- The TLC548 provides low-error conversion of ±0.5 least-significant bit (LSB) in less than 17 microseconds.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} (See Note 1) .... 6.5 V
Input Voltage Range (Any Input) .... −0.3 V to V_{CC+} 0.3 V
Output Voltage Range .... − 0.3 V to V_{CC+} 0.3 V
Operating free-air Temperature Range .... −40°C to 85°C

NOTES: 1. All voltage values are with respect to network ground terminal with the REF- and GND terminal pins connected together, unless otherwise noted.

Overview of Operation

The TLC548 is a complete data acquisition system and it includes such functions as an internal System Clock, Sample-and-hold, 8-bit A/D converter, Data register, Control logic, I/O Clock, and a Chip Select ($\overline{CS}$).

These control inputs and a 3-state data output facilitate serial communications with a microprocessor or minicomputer. A conversion can be completed in a maximum of 17 microseconds, while total access and conversion time is a maximum of 25 microseconds.

The internal System Clock and I/O Clock are used independently and require no special speed or phase relationship. This simplifies the hardware and software control tasks for the device. Because of this independence and the internal generation of the System Clock, the microprocessor and software need only read the previous conversion result and start the conversion with the I/O Clock. The internal System Clock drives the "conversion-crunching" circuitry.

When $\overline{CS}$ is high, the Data Output pin is in a high-impedance condition and the I/O Clock pin is disabled.

This condition allows each of these pins to share a control logic point with its counterpart pin when additional TLC548 devices are used.

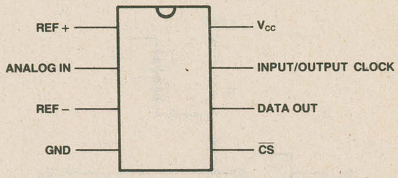
Typical Control Sequence

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result.

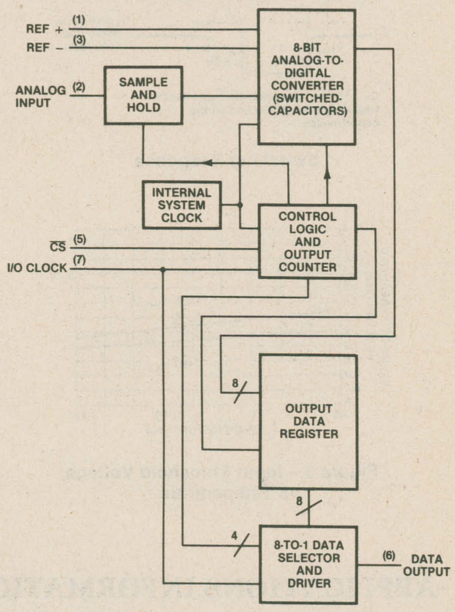
A typical control sequence consists of the following steps.

1. $\overline{CS}$ (Chip Select) is brought low.
   After a $\overline{CS}$ transition (from high to low), the internal circuitry of the TLC548 waits for two rising edges and then one falling edge of the internal System Clock before recognizing the transition. This delay minimizes errors caused by noise at the $\overline{CS}$ input. The most-significant bit (MSB) of the result of the previous conversion then appears on the Data Output pin.
2. The negative edges of the first four I/O Clocks shift out the 2nd, 3rd, 4th, and 5th most-significant bits of the result of the previous conversion.
3. The on-chip sample-and-hold begins sampling the analog input after the 4th falling edge.
   This operation basically involves the charging of internal capacitors to the voltage level of the analog input.

PIN CONNECTION



BLOCK DIAGRAM



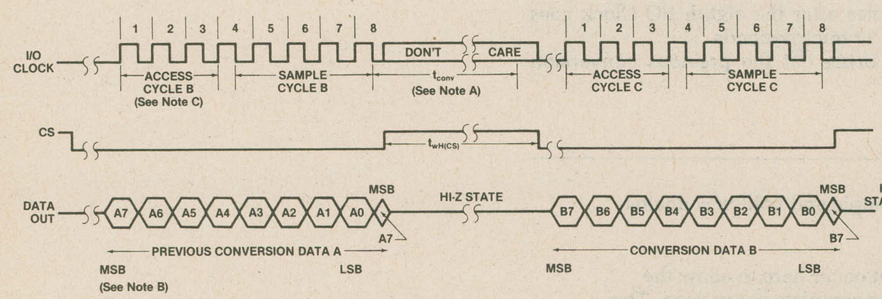
TLC 548 276-1796

Typical Control Sequence (cont.)

4. Three more clock cycles are applied to the I/O pin.
   The 6th, 7th, and 8th bits of the result of the previous conversion are shifted out on the negative edges of these clock cycles.
5. The 8th and final clock cycle is applied to the I/O Clock pin.
   The falling edge of this clock cycle completes the analog sampling process and initiates the hold function.
6. Conversion is performed during the next 36 System Clock cycles.
   After the final I/O Clock cycle, $\overline{CS}$ must go high or the I/O Clock must remain low for at least 36 System Clock cycles to allow for the conversion function.

The operating sequence is illustrated below.

Operating Sequence



NOTES: A. The conversion cycle is initiated with the trailing edge of the 8th I/O Clock pulse after $\overline{CS}$ goes low.

B. The most-significant bit (MSB) is then placed on the DATA OUT pin after $\overline{CS}$ is brought low. The remaining seven bits (A6–A0) are shifted out on the first seven I/O Clock falling edges.

C. To minimize errors caused by noise on the $\overline{CS}$ signal, the internal circuitry waits for two rising edges and then one falling edge of the Internal System Clock (1.4 μs at 2 MHz) after a Chip Select transition before responding to control input signals. Therefore, no attempt should be made to shift out conversion data until the minimum Chip Select setup time has elapsed.

Keeping $\overline{CS}$ Low During Multiple Conversions

$\overline{CS}$ can be kept low during periods of multiple conversions.

If $\overline{CS}$ is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, aborting the conversion in process.

Stopping an Ongoing Conversion

An ongoing conversion can be stopped and a new conversion started by performing steps 1 thru 6 listed under typical control sequence before the 36 System Clock cycles occur. Such an action yields the conversion result of the previous conversion, not the ongoing conversion.

Starting Conversion at a Specific Time

For certain applications such as strobing, it is necessary to start conversion at a specific point in time. The TLC548 will accommodate these applications.

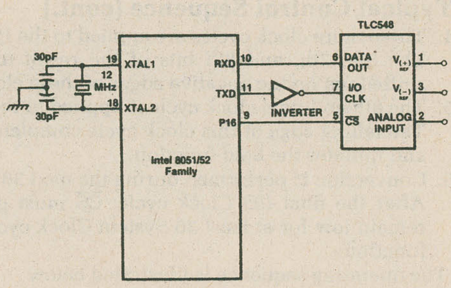
To trigger a conversion at a specific point in time, control hardware or software must manipulate the 8th I/O clock cycle. The sequence for a conversion at a desired instant is:

I. The on-chip sample-and-hold operation waits for the falling edge of the 4th I/O clock cycle and begins sampling. The TLC548 follows the analog input but does not hold it yet.

II. When the 8th I/O clock cycle is high, control hardware or software must keep it high until the desired instant.

III. At the desired instant, control hardware or software must lower the clock. The falling edge of the 8th I/O clock cycle causes the input to be held and initiates the conversion.

TLC 548 276-1796



Intel 8051/52 Serial Port Interface Operating Sequence

The serial data for the conversion result from the TLC548 enters the microprocessor through the RXD pin. By using the inverted TXD shift clock as an I/O Clock for the TLC548, previous conversion data can be transferred to the microprocessor.

The serial port's Mode 0 state is used to permit 8-bit transmission and reception. The TLC548 sends the most-significant bit of the conversion result first; the serial buffer receives this bit as the least-significant bit. The software then reverses the conversion bits and places them in the proper order.

The timing consists of the following three major phases:

1. After $\overline{\text{CS}}$ goes low, eight I/O Clock cycles access and sample the new analog input. At the same time, I/O Clock falling edges bring out the previous conversion result.
2. Conversion begins when the eighth I/O Clock goes low. Conversion requires 36 internal System Clock cycles after the eighth I/O Clock goes low. The maximum conversion time is 17 microseconds.
3. Eight falling edges of the I/O Clock bring out the previous conversion result.

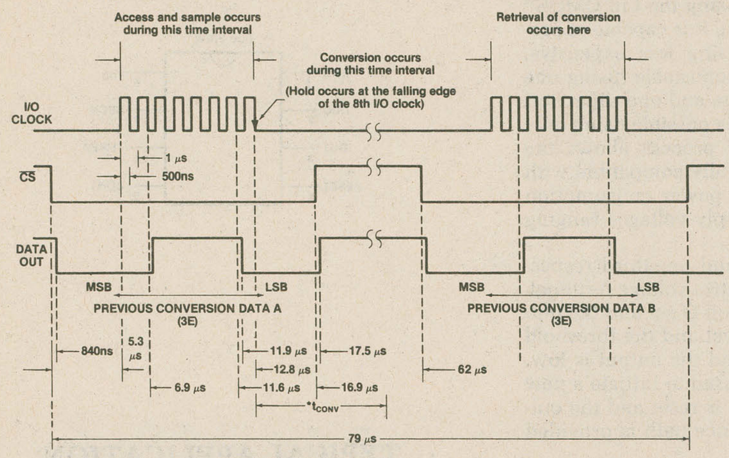
Interface Control Software

```
                          ;
        ACALL SR549D      ; Access, sample and hold new analog
                          ; signal.
                          ;
                          ; Delay must occur here to allow the
                          ; A/D chip to complete conversion. The
                          ; delay must allow 36 A/D chip internal
                          ; System Clock cycles to occur.
                          ; Conversion requires maximum of 17
                          ; microseconds.
                          ;
        ACALL SR549D      ; Access, sample and hold new analog
                          ; signal. Bring out previoous conversion
                          ; result.
                          ; Serial port read reverses data
                          ; conversion bits coming to micro-
                          ; processor so that they are in the following
                          ; order: b0(LSB), b1, b2, b3, b4, b5, b6
                          ; b7(MSB). These bits and Carry bit
                          ; (C) are presented in the following
                          ; instruction comments so the reader
                          ; understands the technique used to
                          ; place bits in proper order.
                          ;
        RLC A             ; 6543210C 7; b7 is now in Carry
        RLC A             ; 543210C7 6; b6 is now in Carry
        MOV ACC.1,C       ; 54321067 6; put b6 into ACC.1
        MOV C,ACC.2       ; 54321067 0; put b0 into C
        RLC A             ; 43210670 5; b5 is now in Carry
        MOV ACC.3,C       ; 43215670 5; put b5 into ACC.3
        MOV C,ACC.4       ; 43215670 1; put b1 into C
        RLC A             ; 32156701 4; b4 is now in Carry
        MOV ACC.5,C       ; 32456701 4; put b4 into ACC.5
        MOV C,ACC.6       ; 32456701 2; put b2 into C
        RLC A             ; 24567012 3; b3 is now in Carry
        MOV ACC.7,C       ; 34567012 3; put b3 into ACC.7
        RL A              ; 45670123  ; prepare for SWAP A
        SWAP A            ; 01234567  ; bits ordered correctly
                          ; Conversion result is in Accumulator
                          ;
                          ; Subroutine ACALL
SR549D  CLR P1.6          ; Lower Chip Select
        ORL SCON,#10H     ; Set REN
        ANL SCON,#FEH     ; Reset R1
        JNB SCON.0,RCV    ; R1 flag not set; branch
                          ; until reception is complete.
        CPL P1.6          ; Raise Chip Select
        RET               ; Conversion is in SBUF
        END               ;
```

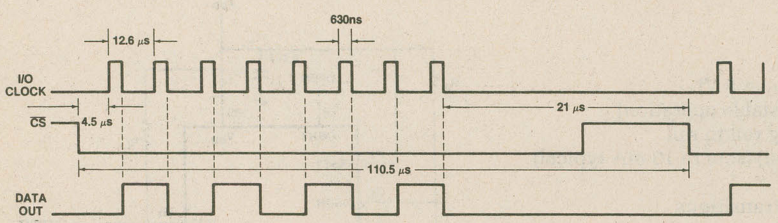
TLC 548 276-1796

The Operating Sequence (cont.)

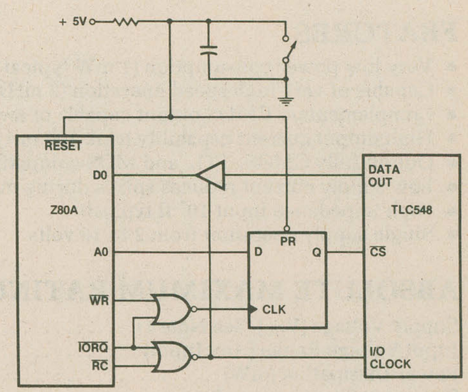
This interface is ideal if the Intel microprocessor's serial port does not have to be used for another purpose. However, if another purpose is required by the serial port, the microprocessor's serial port may be multiplexed so that both the TLC548 and the additional purpose may be accommodated.



Circuit Timing for Intel 8051/52



Microprocessor Interface



Z80A Interface

The Z80A interface is an economical solution, offering efficient control software and communications with the TLC548.

Required Software

A simple program segment that reads in a previous conversion result and starts a conversion is shown below. Placing this program segment in a loop makes it possible to initiate a conversion and read previous conversion results in 111 microseconds.

```
      LD C,08H          ; Load bit counter
      LD B,00H          ; Initialize result register
      OUT (CSLOW) ,A    ; Bring Chip Select low
LOOP  RLC B             ; Rotate result register left
      IN A,(BIT)        ; Read in a bit & shift next
      AND 01H           ; Mask off bit 0
      OR B              ; Or new bit with result
      LD B,A            ; Store in result register
      DEC C             ; Decrement bit counter
      JP NZ,LOOP        ; Get another bit if not zero
      OUT (CSHIGH),A    ; Bring Chip Select high
```

The Operating Sequence

Latching in a low from address bit A0 brings Chip Select low. Execution of an IN instruction causes $\overline{RD}$ and $\overline{IORQ}$ to become active, generating one I/O Clock pulse. A data bit is read in just before the falling edge of the I/O Clock. The falling edge shifts out the next data bit.

Sampling of analog input begins at the falling edge of the 4th I/O Clock and continues until the falling edge of the 8th I/O Clock. At that time, conversion begins; conversion requires 17 microseconds.

$\overline{CS}$ is brought high after the 8th I/O Clock to disable all inputs and outputs so that conversion may proceed undisturbed.

TLC555 TIMER
276-1718

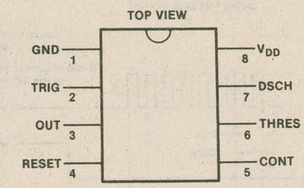
GENERAL DESCRIPTION

The TLC555 is a monolithic timing circuit fabricated using the Lin CMOS™ process. Due to its high-impedance inputs (typically $10^{12}\Omega$), it is capable of producing accurate time delays and oscillations while using less expensive, smaller timing capacitors. The TLC555 achieves both monostable (using one resistor and one capacitor) and astable (using two resistors and one capacitor) operation. In addition, 50% duty cycle astable operation is possible using only a single resistor and one capacitor. The Lin CMOS™ process allows the TLC555 to operate at frequencies up to 2 MHz and be fully compatible with CMOS, TTL, and MOS logic. It also provides very low power consumption (typically 1 mW at V_{DD} = 5V) over a wide range of supply voltages ranging from 2 volts to 18 volts.

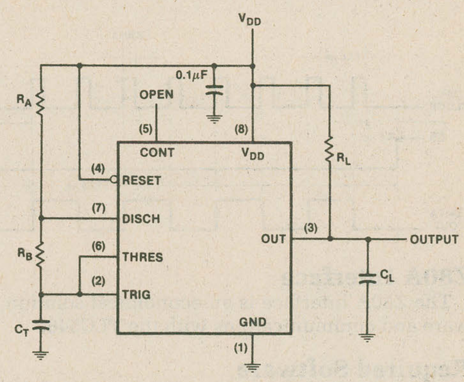
Threshold and trigger levels are normally two-thirds and one-third respectively of V_{DD}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low impedance path is provided between the discharge terminal and ground.

While the complementary CMOS OUTPUT is capable of sinking over 100 mA and sourcing over 10 mA, the TLC555 exhibits greatly reduced supply current spikes during output transitions.

PIN CONNECTION



TYPICAL APPLICATION



Circuit for Astable Operation

FEATURES

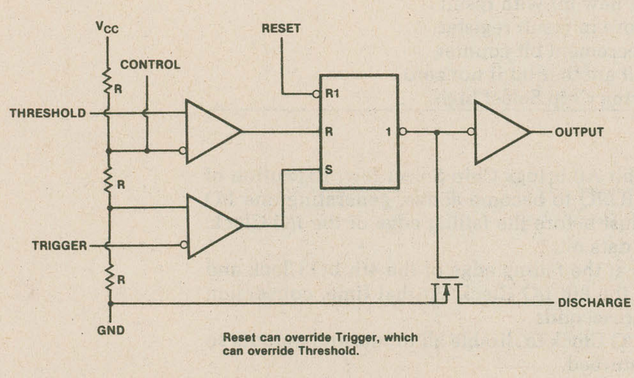
- Very low power consumption (1 mW typical at V_{DD} = 5 V)
- Capable of very high-speed operation (2 mHz in a stable operation)
- Complementary CMOS output capable of swinging rail to rail
- High output-current capability (sink 100 mA typical) (soucre 10 mA typical)
- Output fully CMOS, TTL, and MOS-compatible
- Low supply current reduces spikes during output transitions
- High impedance input $10^{12}\Omega$ typical)
- Single supply operation from 2 to 18 volts

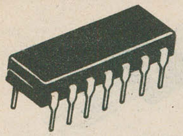
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD}) (See Note 1)	18 V
Input Voltage Range (Any Input)	−03 V To 18 V
Power Dissipation (mW)	600mW
Operating Temperature Range	0°C To 70°C
Storage Temperature Range	−65°C To 150°C

NOTES: 1. All voltage values are with respect to network ground terminal.

BLOCK DIAGRAM





DUAL TIMERS TLC556
276-1704

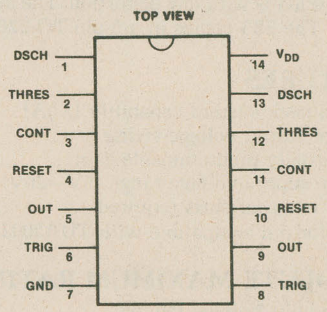
GENERAL DESCRIPTION

The TLC556 is a dual monolithic timing circuit fabricated using the LinCMOS™ process. Due to its high-impedance input (typically $10^{12}\Omega$), it is capable of producing accurate time delays and oscillations while using less expensive, smaller timing capacitors. It achieves both monostable (using one resistor and one capacitor) and astable (using two resistors and one capacitor) operation. In addition, 50% duty cycle astable operation is possible using only a single resistor and one capacitor. The LinCMOS™ process allows the TLC556 to operate at frequencies up to 2 MHz and be fully compatible with CMOS, TTL, and MOS logic. It also provides very low power consumption (typically 2 mW at V_{DD} = 5V) over a wide range of supply voltages ranging from 2 volts to 18 volts.

The threshold and trigger levels are normally two-thirds and one-third respectively of V_{DD}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low impedance path is provided between the discharge terminal and ground.

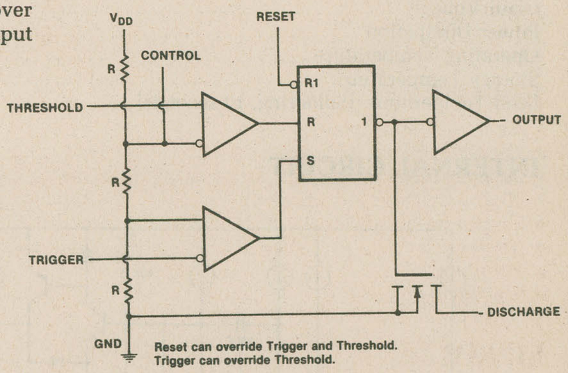
While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA the TLC556 exhibit greatly reduced supply current spikes during output transitions. This minimizes the need for the large decoupling capacitors.

PIN CONNECTION



FEATURES

- Very Low Power Consumption
  2mW Typ at V_{DD} = 5V
- Capable of Very High-Speed Operation Typically 2 MHz in Astable Mode
- Complementary MOS output Capable of Swinging Rail-to-Rail
- High Output-Current Capability
  Sink 100 mA TYP
  Source 10 mA Typ
- Output Fully CMOS-, TTL-, and MOS- Compatible
- Low Supply Current Reduces Spikes During Output Transitions
- High Impedance Inputs $10^{12}\Omega$ Typ
- Single Supply Operation



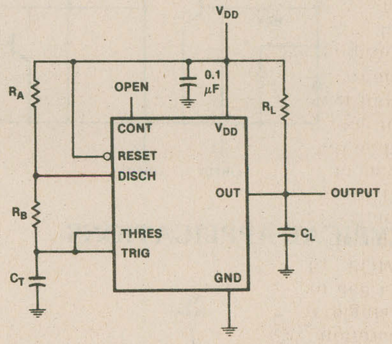
Block Diagram (Each Timer)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD} 18V
Operating Voltage .... 2V to 15V
Input Voltage Range (Any Input) .... -0.3 to 18V
Power Dissipation 950mW
Operating Temperature Range .... 0°C to 70°C
Storage Temperature Range .... -65°C to +150°C

OPERATING CHARACTERISTICS

Initial Error of Timing Interval (V_{DD} = 2 to 15V) 1%
($R_A = R_B$ = 1KΩ to 100KΩ)
(CT = 0.1uF)
Supply Voltage Sensitivity of Timing Interval (V_{DD} = 2 to 15V) 0.1%/V
($R_A = R_B$ = 1KΩ to 100KΩ)
(CT = 0.1uF)
Output Pulse Rise Time V_{DD} = 5V R_L = 10mΩ 20ns
Fall Time CL = 10pF 20ns
Maximum Frequency in Astable Mode R_A = 470Ω R_BB = 200Ω 2.1MHz
CT = 200pF



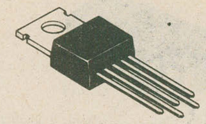
Circuit for Astable Operation

TRUTH TABLE

RESET	TRIGGER VOLTAGE	THRESHOLD VOLTAGE	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< ⅓ V_{DD}	Irrelevant	High	Off
High	> ⅓ V_{DD}	> ⅔ V_{DD}	Low	On
High	> ⅓ V_{DD}	< ⅔ V_{DD}	As previously established	

383
276-703

8 WATT AUDIO POWER AMPLIFIER



GENERAL DESCRIPTION

The 383 is a cost effective, high power amplifier suited for automotive applications. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The 383 is current limited and thermally protected. The 383 comes in a 5-pin TO-220 package.

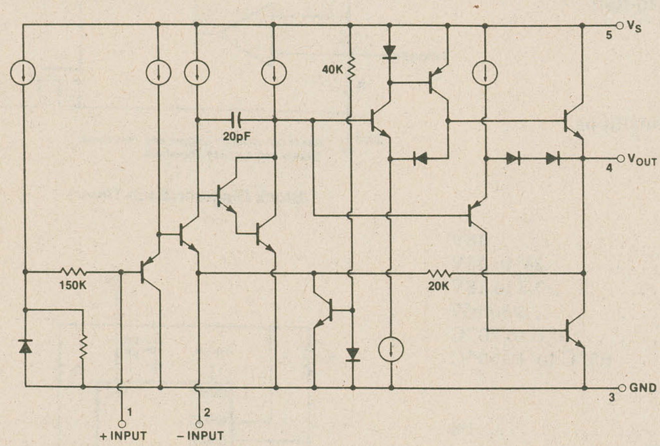
FEATURES

- High peak current capability (3.5A)
- Large output voltage swing
- Externally programmable gain
- Wide supply voltage range (5V—20V)
- Few external parts required
- Pin for pin compatible with TDA2002
- Low distortion
- High input impedance
- No turn-on transients
- Low noise
- Short circuit protected

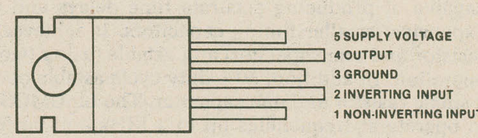
ABSOLUTE MAXIMUM RATINGS

Peak Supply Voltage (50 ms)	25V
Operating Supply Voltage	20V
Output Current	
Repetitive	3.5A
Non-repetitive	4.5A
Input Voltage	±0.5V
Power Dissipation	15W
Operating Temperature	0 to +70°C
Storage Temperature	−60 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

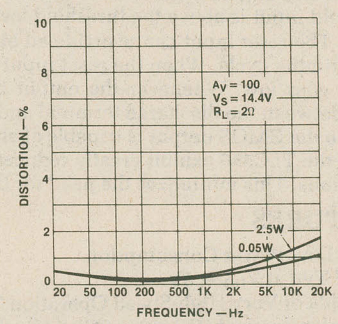
INTERNAL CIRCUIT



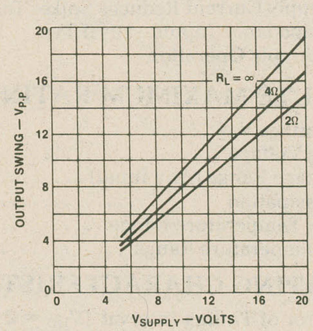
PIN CONNECTION



TYPICAL CHARACTERISTICS

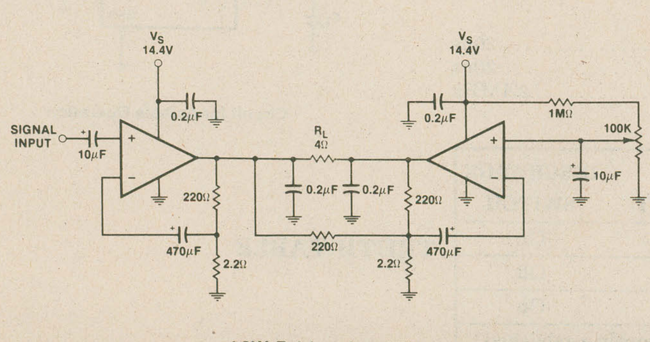


Distortion vs Frequency

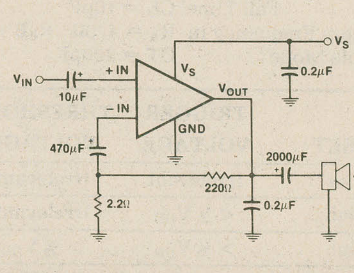


Output Swing vs Supply Voltage

TYPICAL APPLICATIONS



16W Bridge Amplifier



Basic Audio Amp

LOW VOLTAGE AUDIO POWER AMPLIFIER

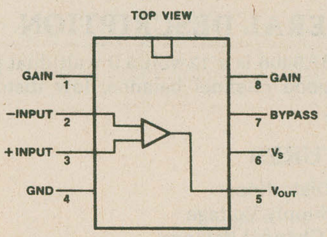
386
276-1731

GENERAL DESCRIPTION

The 386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 18 milli-watts when operating from a 6 volt supply, making the 386 ideal for battery operation.

PIN CONNECTION



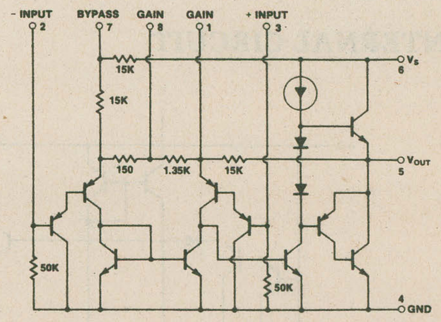
FEATURES

- Battery operation
- Minimum external parts
- Wide supply voltage range 4-12 volts
- Low quiescent current drain 3 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Eight pin dual-in-line package

APPLICATIONS

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

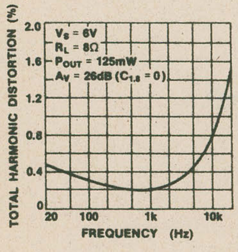
INTERNAL CIRCUIT



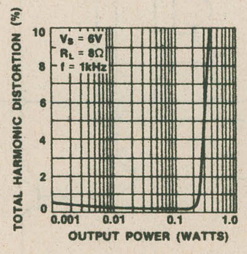
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15V
Package Dissipation 8 Pin DIP	660 mW
Input Voltage	±0.4V
Junction Temperature	+150°C
Operating Temperature	0 to +70°C
Storage Temperature	−65 to +150°C
Lead Temperature (Soldering. 10 seconds)	+300°C

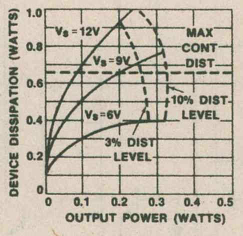
TYPICAL CHARACTERISTICS



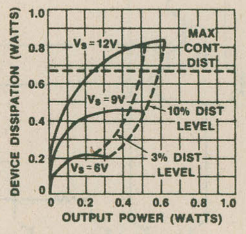
Distortion vs Frequency



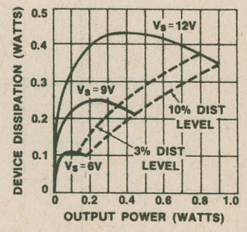
Distortion vs Output Power



Device Dissipation vs Output Power—4Ω Load

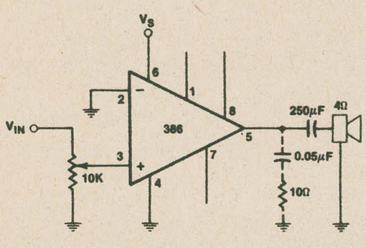


Device Dissipation vs Output Power—8Ω Load

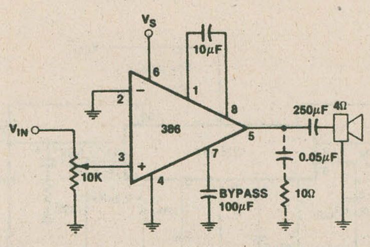


Device Dissipation vs Output Power—16Ω Load

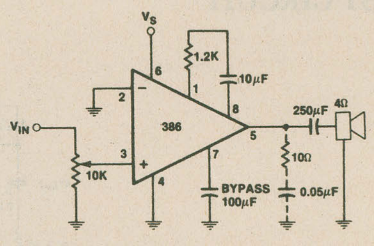
TYPICAL APPLICATIONS



Amplifier with Gain = 20 (Minimum Parts)



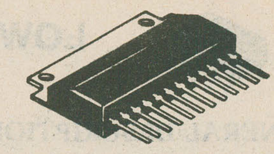
Amplifier with Gain = 50



Amplifier with Gain = 200

BA5406
276-707

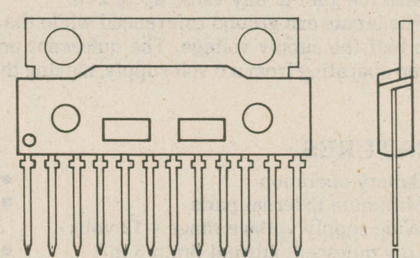
DUAL POWER AMP



GENERAL DESCRIPTION

The BA5406 is a 12 volt 5.0 watt dual power amplifier featuring less pop up noise, good channel balance, low distortion and operates at a low supply voltage.

PIN CONNECTION



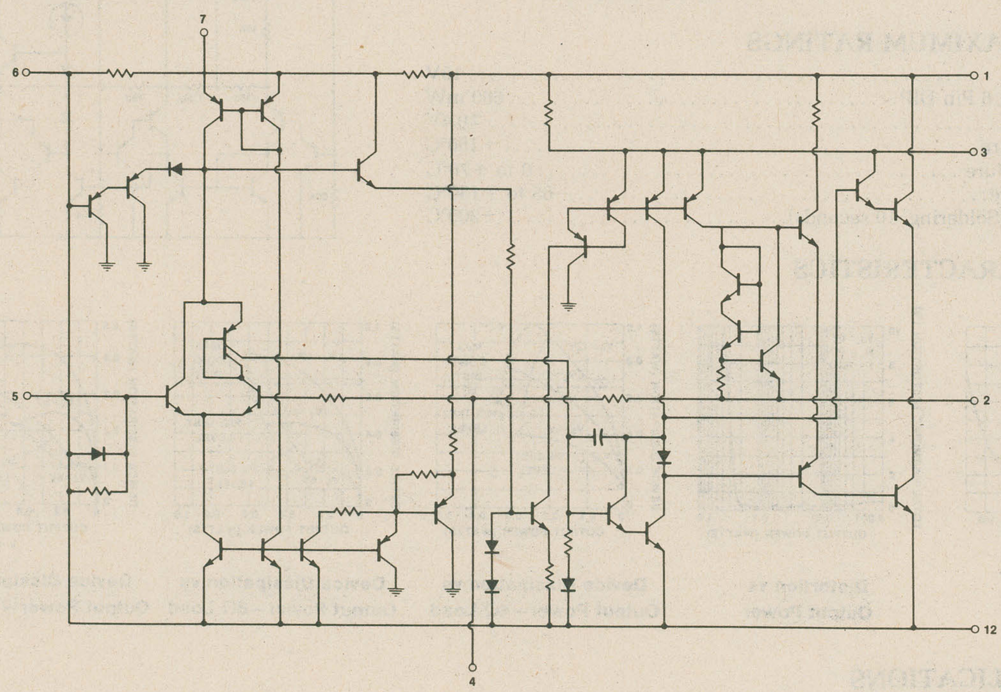
FEATURES

- Low Distortion
- Low Supply Voltage
- Good Channel Balance
- Less Pop Up Noise

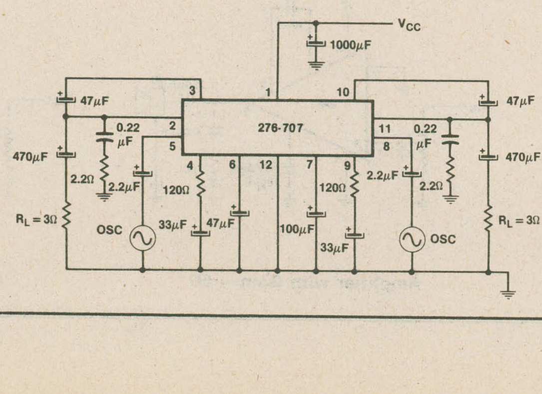
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (V_{CC}) (V_{IN} = OV) 18V
Operating Voltage (V_{CC})... .5V to 15V
Power Dissipation (P_D) (Back Metal Temp = 75°C) 20W
Operating Temperature .... −20 to +75°C
Storage Temperature.. −30 to +125°C

INTERNAL CIRCUIT

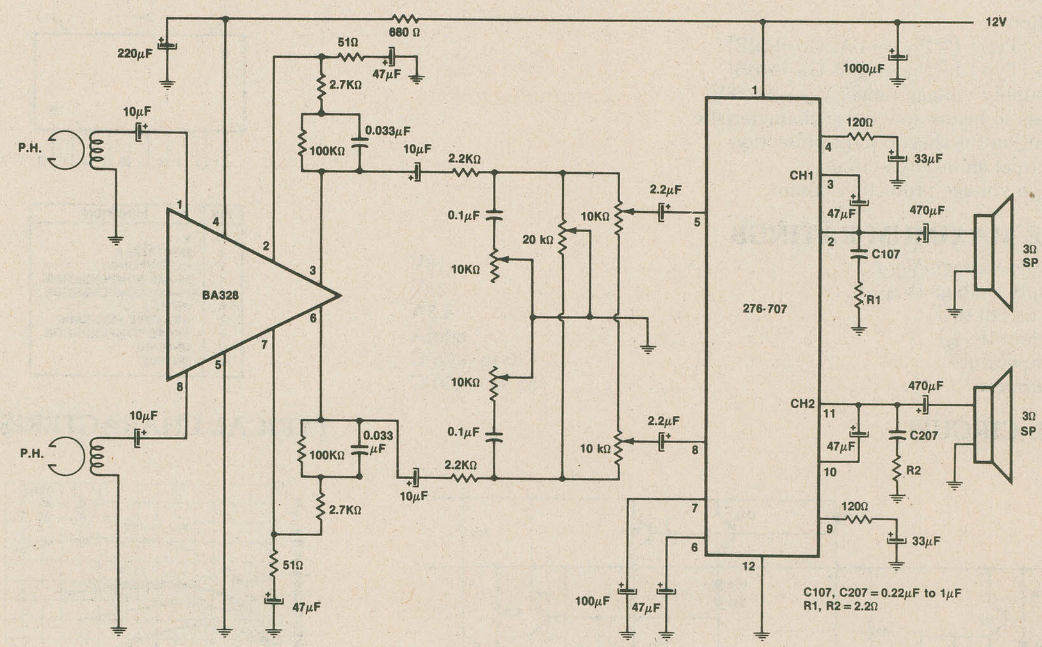


TEST CIRCUIT

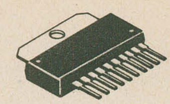


BA5406 276-707

TYPICAL APPLICATION



TA7205AP 276-705 5.8W AUDIO POWER AMPLIFIER



GENERAL DESCRIPTION

The TA7205AP is a monolithic audio power amplifier with a built in thermal shut-down circuit designed for car radio and stereo applications.

FEATURES

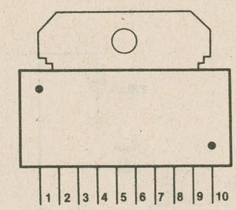
- Low distortion
  THD=0.15% (Typ.) (@P_{OUT}=1W, G_V=55dB)
  THD=0.07% (Typ.) (@P_{OUT}=1W, G_V=44dB)
- Operating supply voltage range: V_{CC}=9∼18V
- 'PCT' process to insure low noise characteristic
- Current limiting for short-circuit protection
- Built in thermal shut-down circuit
- Built in surge voltage protection circuit

ABSOLUTE MAXIMUM RATINGS

Operating Supply Voltage(V_{CC}) 18V
Quiescent Supply Voltage (V_{CCQ}) 25V
Output Peak Current (I_O) 4.5A
Quiescent Current (I_{CCQ}) 80mA
Operating Temperature .... −20 to +75°C
Storage Temperature .... −55 to +150°C

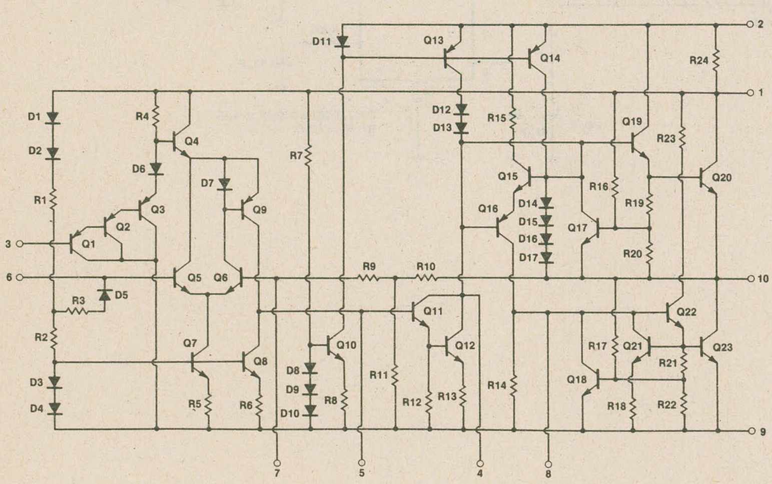
PIN CONNECTION

FRONT VIEW

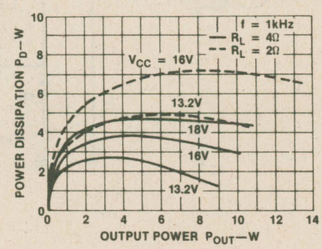


PIN	FUNCTION
1	V+
2	BOOTSTRAP
3	DECOUPLING
4	PHASE COMPENSATION
5	PHASE COMPENSATION
6	INPUT
7	NEGATIVE FEEDBACK
8	PHASE COMPENSATION
9	GROUND
10	OUTPUT

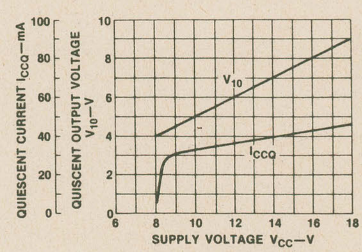
INTERNAL CIRCUIT



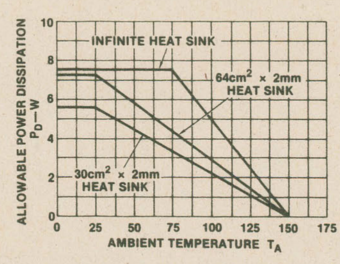
TYPICAL CHARACTERISTICS



Power Dissipation vs Output Power

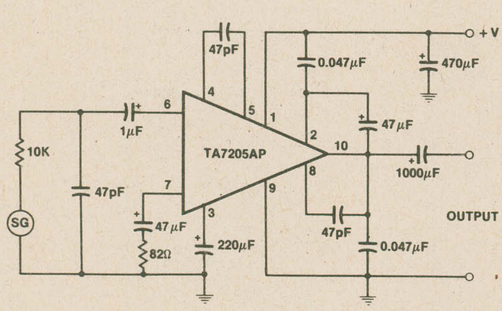


Quiescent Current and Output Voltage vs Supply Voltage

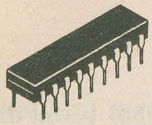


Allowable Power Dissipation vs Ambient Temperature

TYPICAL APPLICATION



5 Watt Audio Amplifier



DOT/BAR DISPLAY DRIVER

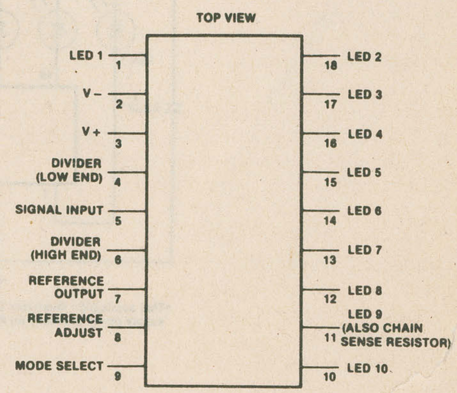
3914
276-1707

GENERAL DESCRIPTION

The 3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating resistors. This feature allows operation of the system from less then 3V. Controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many 3914s can be "chained" to form displays of segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

Individual DC regulated currents provide flexibility and various effects can be achieved by modulating these currents. Outputs can drive a transistor and a LED so controller functions including "staging" control can be performed.

PIN CONNECTION



FEATURES

- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 to 3 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic. The internal 10-step divider is floating and can be reference to a wide range of voltages

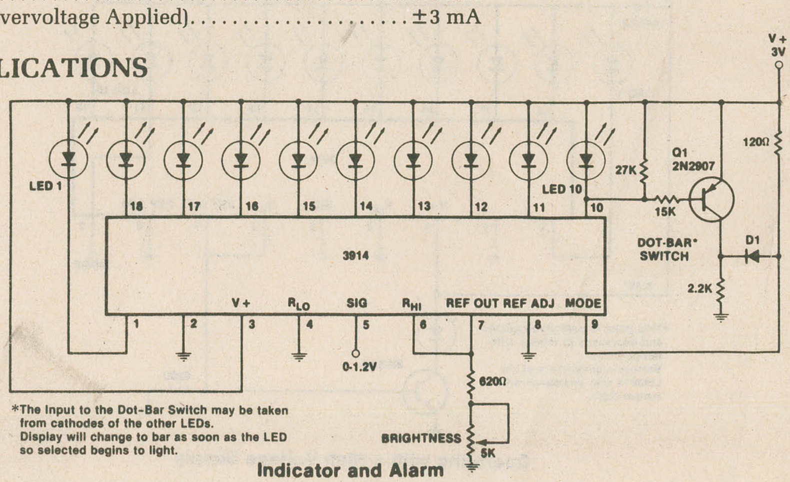
APPLICATIONS

- "Slow"—fade bar or dot display (doubles resolution)
- 20 step meter with single pot brightness control
- 10-step (nor multiples) programmer
- Multi-step or "staging" controller
- Combined controller and process deviation meter
- Exclamation point display for power savings
- Power Meters in stereo systems
- VU Meters in tape recorders
- S meters in Ham and CB radios
- Direction and rate indicator (to add to DVMs)

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	660 mW
V + Voltage	25V
LED Collector Output Voltage	25V
Input Signal Overvoltage	±35V
Voltage on Resistor String	−100 MV to V+
Reference Load Current	10 mA
Signal Input Current (With Overvoltage Applied)	±3 mA

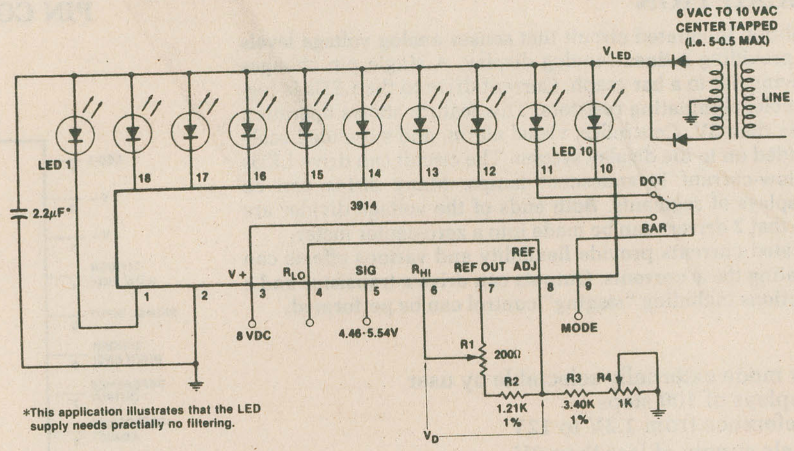
TYPICAL APPLICATIONS



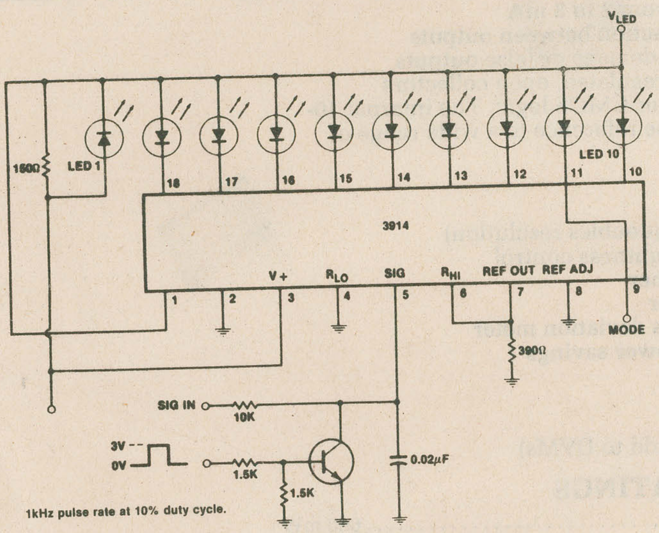
Indicator and Alarm

3914 276-1707

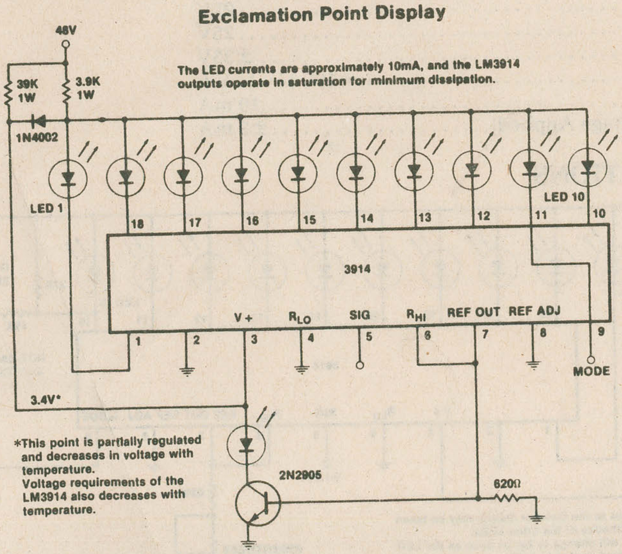
TYPICAL APPLICATIONS (Cont'd)



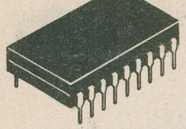
Expanded Scale Meter, Dot or Bar



Exclamation Point Display



Operating with a High Voltage Supply



DOT/BAR DISPLAY DRIVER

3916
276-1709

GENERAL DESCRIPTION

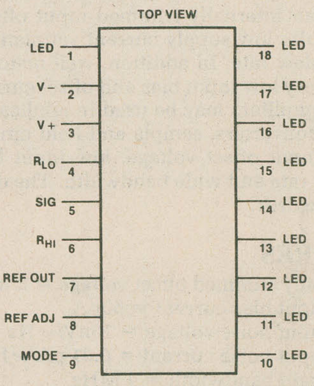
The 3916 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing an electronic version of the popular VU meter. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 0.2 dB.

Audio applications include average or peak level indicators, and power meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

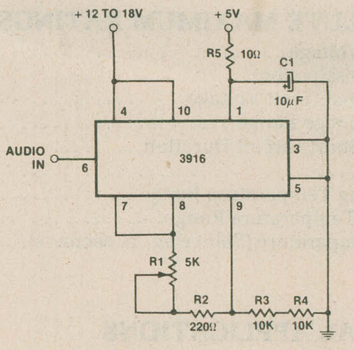
The 3916 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

PIN CONNECTION



FEATURES

- Fast responding electronic VU meter
- Drives LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 70 dB
- Internal voltage reference from 1.2V to 12V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

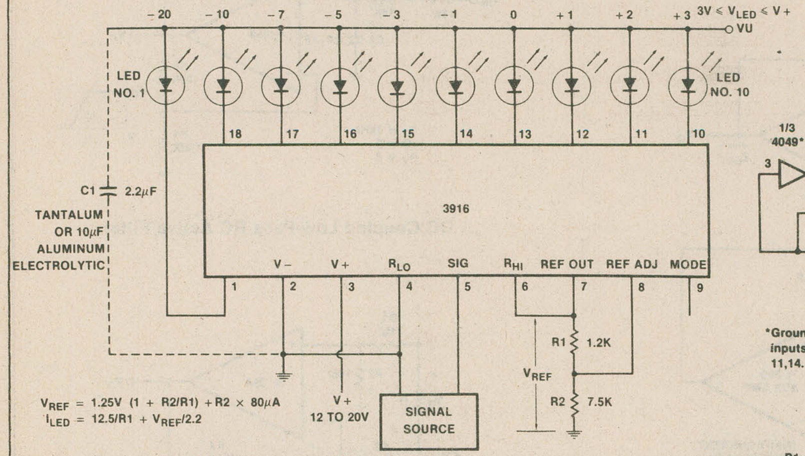


VU Bar Graph Display

ABSOLUTE MAXIMUM RATINGS

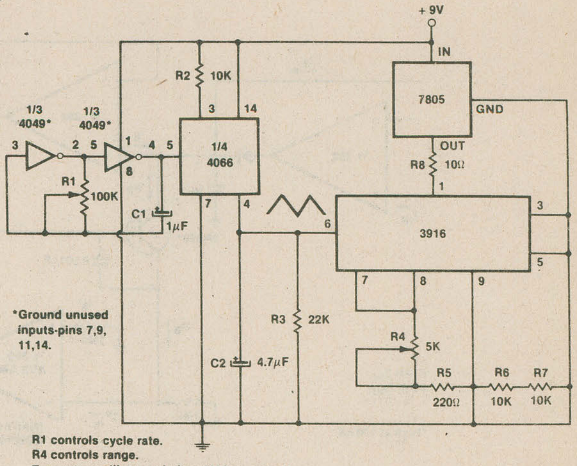
Supply Voltage .... 3 to 25 V
Input Signal Over Voltage .... ± 35 V
Storage Temperature .... 0 to 70°C

TYPICAL APPLICATIONS



Notes: 1. Capacitor C1 is required if leads to the LED supply are 6" or longer.
2. Circuit as shown is wired for dot anode. For bar mode, connect pin 9 to pin 3.
I_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

0V to 10V VU Meter



R1 controls cycle rate.
R4 controls range.
Two gate oscillator switches 4066 on and off.
C2 is charged via R2 and discharged by R3 to give voltage ramp.

Back and Forth Flasher

353
276-1715

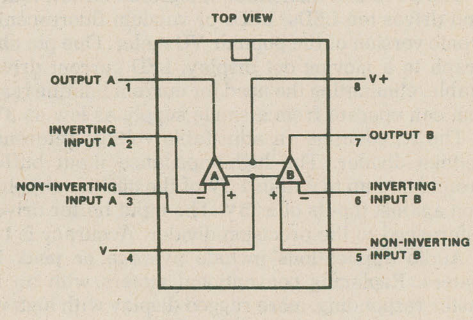
WIDE BANDWIDTH DUAL JFET INPUT OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™) technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents.

These amplifers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

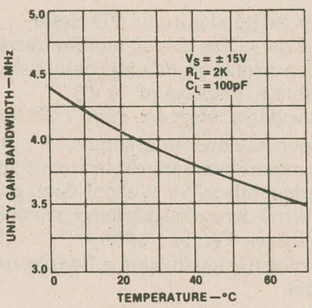
PIN CONNECTION



FEATURES

- Internally trimmed offset voltage = 2 mV
- Low input bias current = 50pA
- Low input noise voltage = 16nV/√Hz
- Low input noise current = 0.01 pA/√Hz
- Wide gain bandwidth = 4 MHz
- High slew rate = 13 V/μs
- Low supply current = 3.6 mA
- High input impedance = $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz—20kHz = <0.02%
- Low 1/f noise corner = 50 Hz
- fast settling time to 0.0% = 2μs

TYPICAL CHARACTERISTICS

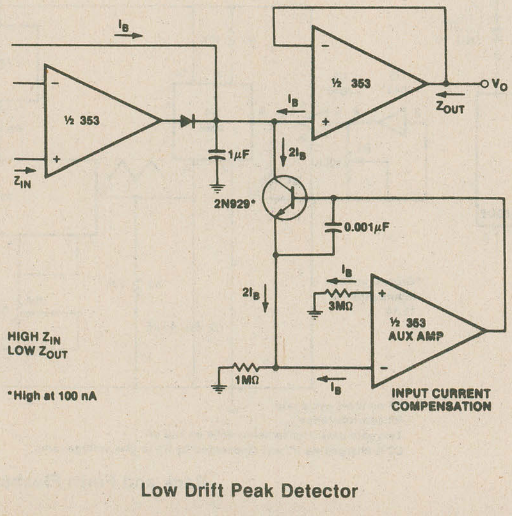


Unity Gain Bandwidth vs Temperature

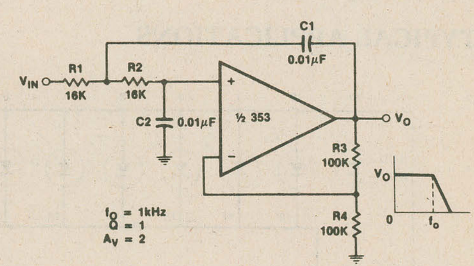
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation	500 mW
Differnetial Input Voltage	±30V
Input Voltage Range	±15V
Output Short Circuit Duration	Continuous
$T_{j(MAX)}$	115°C
Operating Temperature Range	0 to 70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

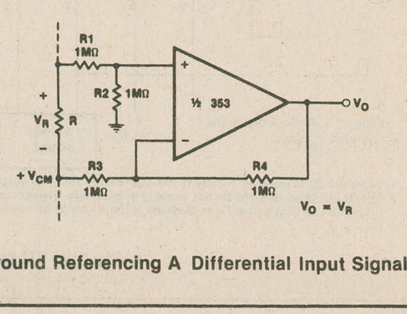
TYPICAL APPLICATIONS



Low Drift Peak Detector

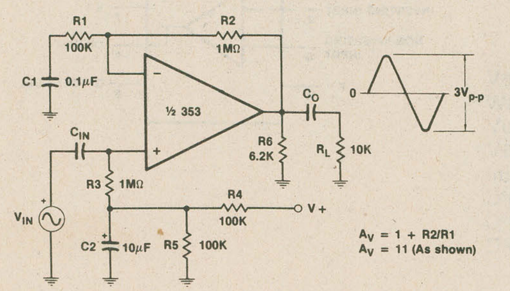


DC Coupled Low-Pass RC Active Filter

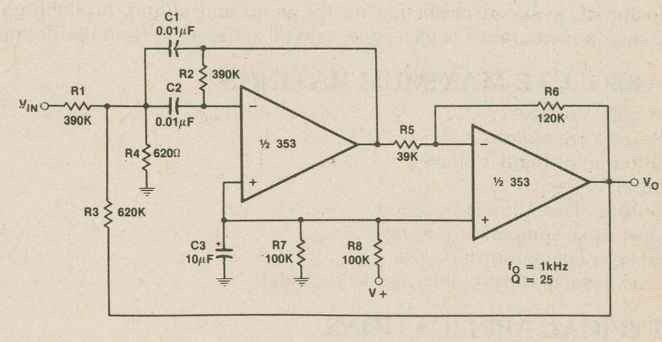


Ground Referencing A Differential Input Signal

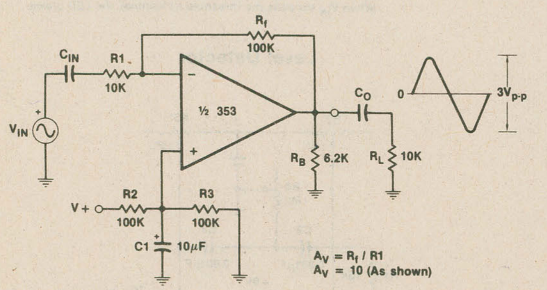
TYPICAL APPLICATIONS (Cont'd)



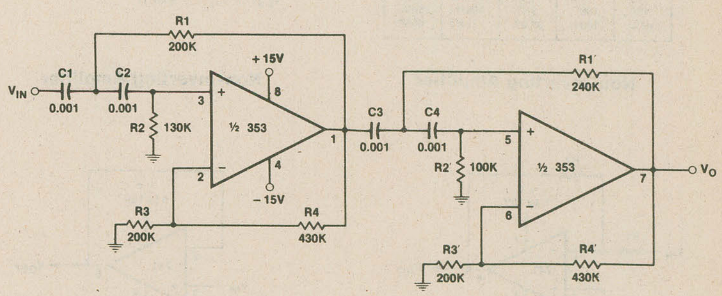
AC Coupled Non-Inverting Amplifier



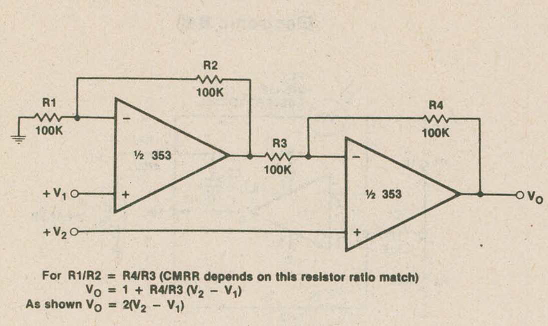
Bandpass Active Filter



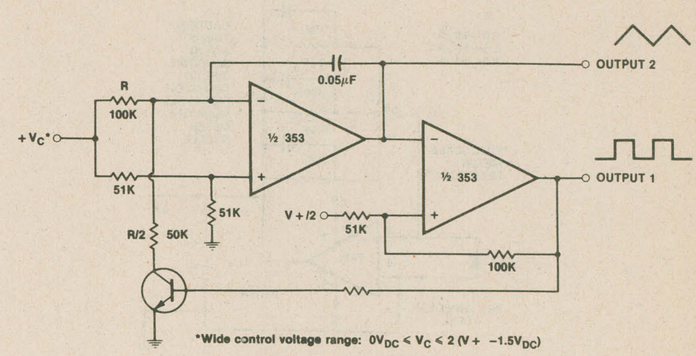
AC Coupled Inverting Amplifier



Fourth Order High Pass Butterworth Filter



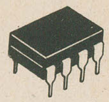
High Input Z, DC Differential Amplifier



Voltage Controlled Oscillator (VCO)

741
276-007

OPERATIONAL AMPLIFIER

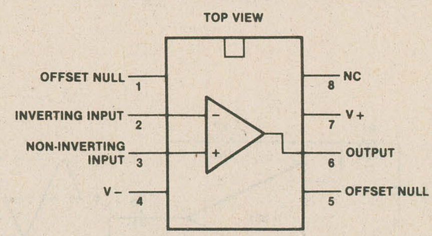


GENERAL DESCRIPTION

The 741 series are general purpose operational amplifiers which feature improved performance over industry standards.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

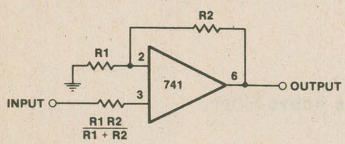
PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

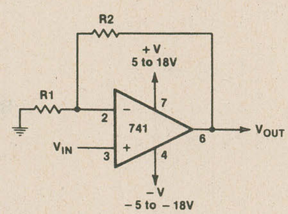
Supply Voltage .... ±16V
Power Dissipation .... 500 mW
Differential Input Voltage .... ±30V
Input Voltage .... ±15V
Output Short Circuit Duration .... Indefinite
Operating Temperature Range .... 0 to +70°C
Storage Temperature Range .... −65 to +150°C
Lead Temperature (Soldering, 10 seconds) .... 300°C

TYPICAL APPLICATIONS



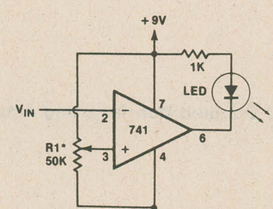
GAIN	R1	R2	BW	R_{IN}
10	1K	9K	100kHz	400MΩ
100	100Ω	9.9K	10kHz	280MΩ
1000	100Ω	99.9K	1kHz	80MΩ

Non-Inverting Amplifier



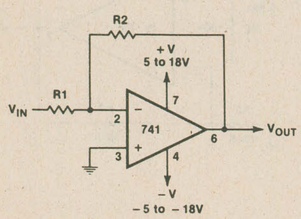
$V_{OUT} = V_{IN} (1 + R2/R1)$

Non-Inverting Amplifier



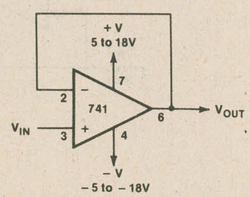
*R1 sets the voltage detection threshold (up to +9V). When V_{IN} exceeds the threshold (reference), the LED glows.

Level Detector



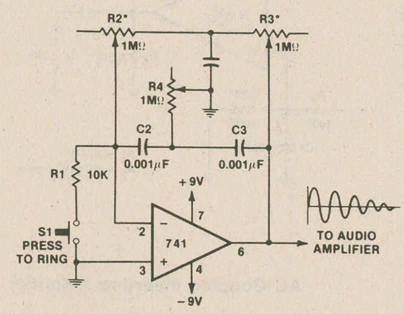
$V_{OUT} = -V_{IN} (R2/R1)$

Inverting Amplifier



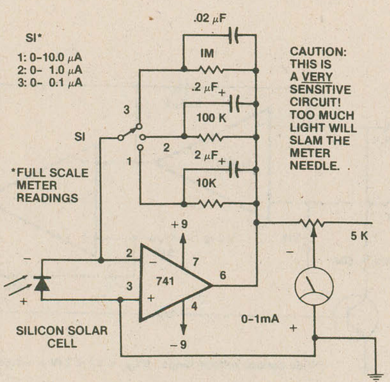
$V_{OUT} = V_{IN}$

Unity Gain Follower

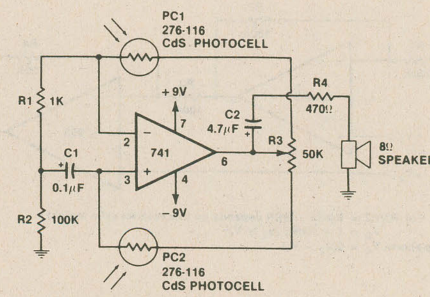


*Adjust R3 to just below oscillation point. Adjust R2 and R3 for sounds such as bell, drum, tinkling, etc.

Electronic Bell

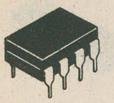


Optical Power Meter



Light on PC1 decreases tone frequency
Light on PC2 increases tone frequency

Audible Light Sensor



DUAL OPERATIONAL AMPLIFIER

1458
276-038

GENERAL DESCRIPTION

The 1458 is a general purpose dual operational amplifier. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

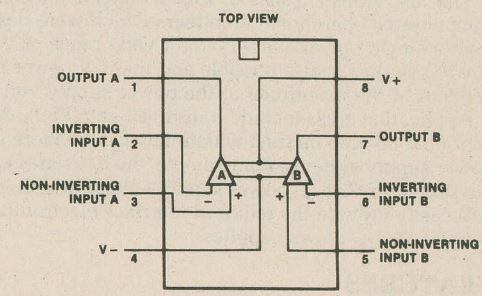
FEATURES

- No frequency compensation required.
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- No latch up when input common mode range is exceeded

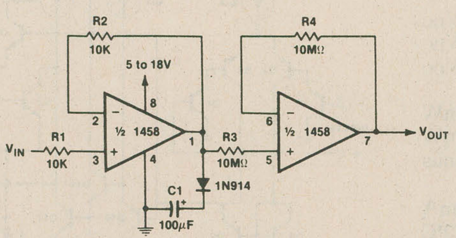
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±16V
Power Dissipation	400 mW
Differential Input Voltage	±30V
Input Voltage	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

PIN CONNECTION

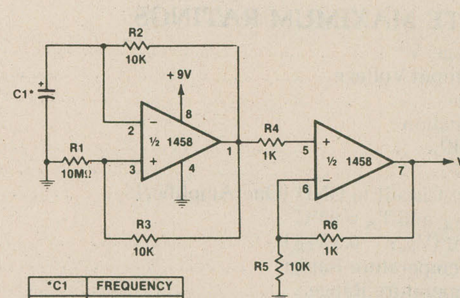


TYPICAL APPLICATIONS



C1 stores the peak voltage at V_{IN}.

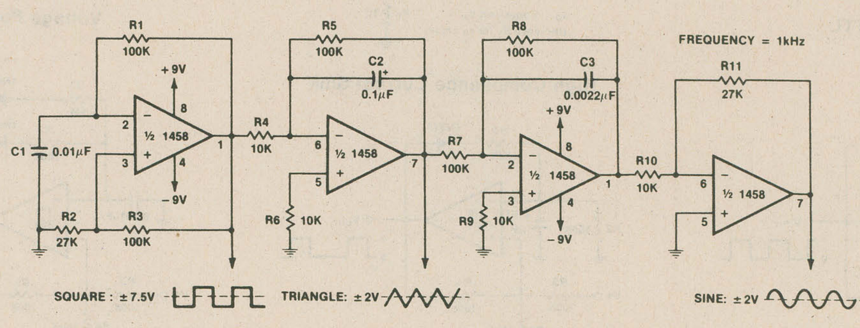
Peak Detector



*C1	FREQUENCY
0.001μF	5872Hz
0.010μF	660Hz
0.100μF	51Hz
1.000μF	8Hz

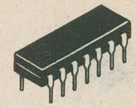
Pulses are DC when C1 = 0.1μF
Amplitude is 5 volts.

Pulse Generator



Function Generator

324 276-1711 QUAD OP AMP



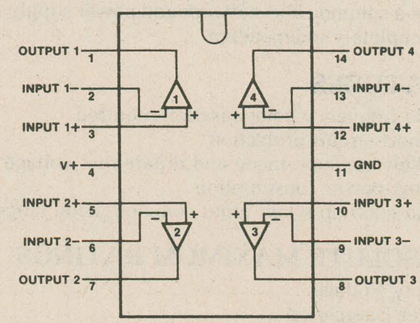
GENERAL DESCRIPTION

The 324 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the 324 series can be directly operated off of the standard $+5\ V_{DC}$ power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $+15\ V_{DC}$ power supplies.

PIN CONNECTION

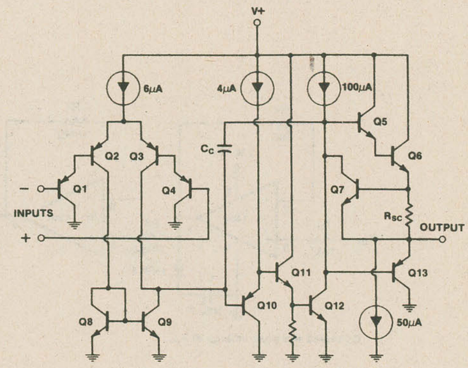
TOP VIEW



FEATURES

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  Single supply 3 V_{DC} to 30 V_{DC}
  or dual supplies $\pm 1.5\ V_{DC}$ to $\pm 15\ V_{DC}$
- Very low supply current drain (800 μA)—essentially independent of supply voltage (1 mW/op amp at $+5\ V_{DC}$)
- Low input biasing current 45 nA_{DC} (temperature compensated)
- Low input offset voltage 2 mV_{DC} and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to $V^+ - 1.5\ V_{DC}$

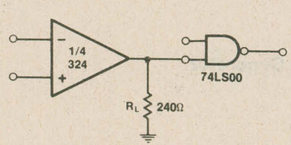
INTERNAL CIRCUIT (Each Amplifier)



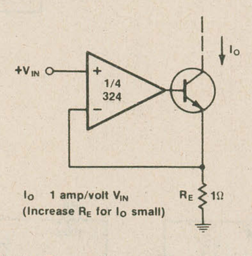
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V^+	32 V_{DC} or $\pm 16\ V_{DC}$
Differential Input Voltage	32 V_{DC}
Input Voltage	$-0.3\ V_{DC}$ to $+32\ V_{DC}$
Power Dissipation	
Molded DIP	570 mW
Cavity DIP	900 nW
Output Short-Circuit to GND (One Amplifier) $V^+ \leq 15\ V_{DC}$ and $T_A = 25°C$	Continuous
Input Current ($V_{IN} < -0.3\ V_{OL}$)	50 mA
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

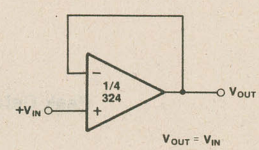
TYPICAL APPLICATIONS



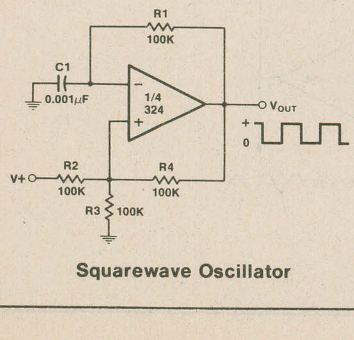
Driving TTL



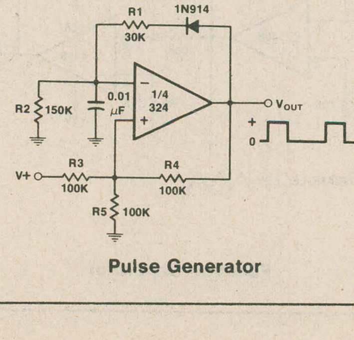
High Compliance Current Sink



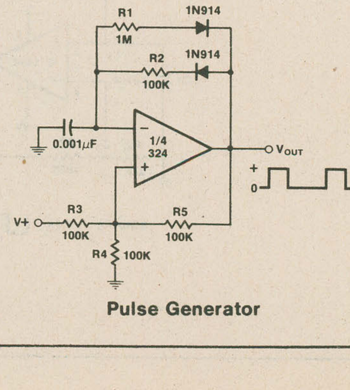
Voltage Follower



Squarewave Oscillator



Pulse Generator



Pulse Generator

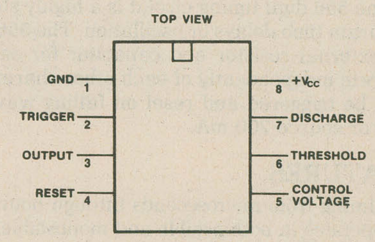
TIMER

555
276-1723

GENERAL DESCRIPTION

The 555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

PIN CONNECTION



FEATURES

- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

TRUTH TABLE

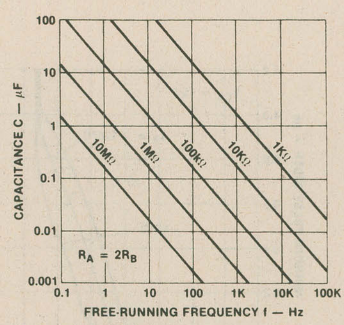
PIN 2 TRIGGER	PIN 6 THRESHOLD	PIN 4 RESET	PIN 3 OUTPUT
H	X	H	L
L	X	H	H
H	L	H	L
X	X	L	L

X = Don't Care L = Low Level H = High Level

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +16V
Power Dissipation .... 600 mW
Operating Temperature Range .... 0 to +70°C
Storage Temperature Range .... −65 to +150°C
Lead Temperature (Soldering, 10 seconds) .... 300°C

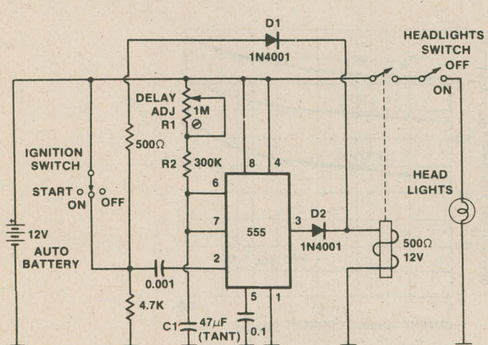
TYPICAL CHARACTERISTICS



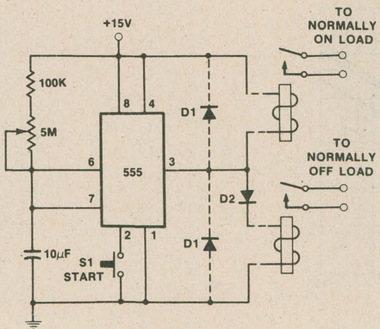
Capacitance vs Free-Running Frequency

The charge time (output high) is given by: $t_1 = 0.693\ (R_A + R_B)\ C$
The discharge time (output low) is given by: $t_2 = 0.693\ (R_B)\ C$
Thus the total period is: $T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$
The frequency of oscillation is: $f = 1/T = 1.44\ /\ (R_A + 2R_B)\ C$

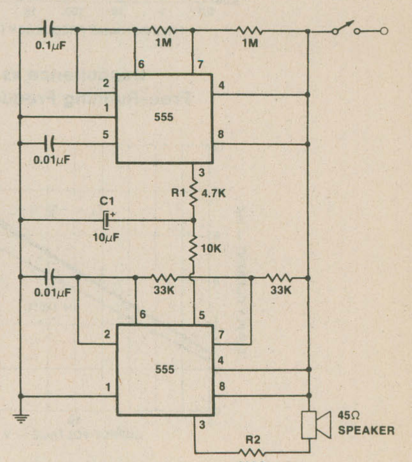
TYPICAL APPLICATIONS



Automatic Headlight Turn-Off Circuit



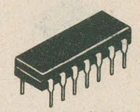
Relay Timer



Warble Alarm Circuit

556
276-1728

DUAL TIMER

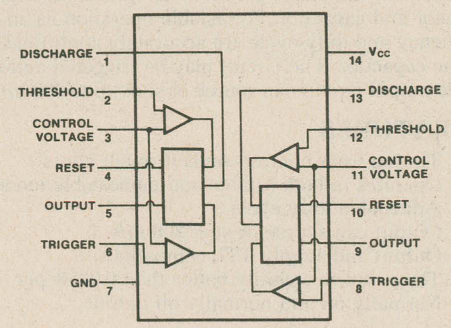


GENERAL DESCRIPTION

The 556 dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

PIN CONNECTION

TOP VIEW



FEATURES

- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

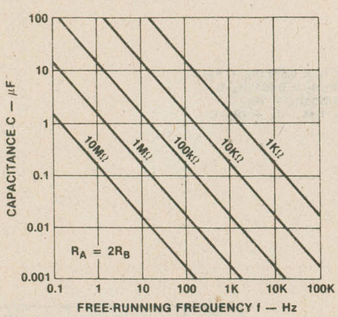
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

ABSOLUTE MAXIMUM RATINGS

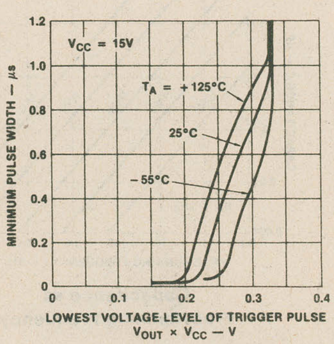
Supply Voltage	+16V
Power Dissipation	600 mW
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TYPICAL CHARACTERISTICS

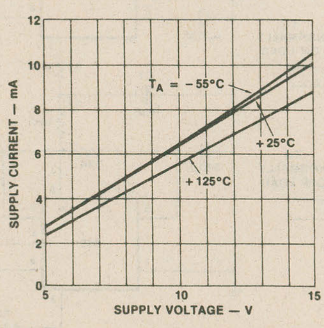


Capacitance vs Free-Running Frequency

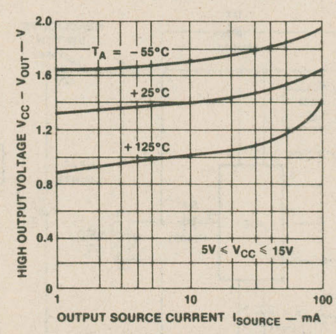
The charge time (output high) is given by:
$t_1 = 0.693\ (R_A + R_B)\ C$
The discharge time (output low) is given by:
$t_2 = 0.693\ (R_B)\ C$
Thus the total period is:
$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$
The frequency of oscillation is:
$f = 1/T = 1.44\ /\ (R_A + 2R_B)\ C$



Minimum Pulse Width vs Lowest Voltage Level of Trigger Pulse



Supply Current vs Supply Voltage



High Output Voltage vs Output Source Current

3-TERMINAL ADJUSTABLE POSITIVE REGULATOR

317T
276-1778

GENERAL DESCRIPTION

The 317T is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 1.5 A over a 1.2 V to 37 V output range. This device is exceptionally easy to use and requires only two external resistors to set the output voltage.

In addition to higher performance than fixed regulators, the 317T offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

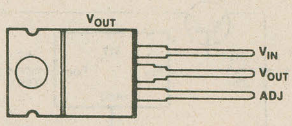
Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

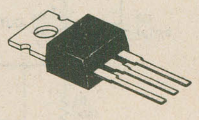
Besides replacing fixed regulators, the 317T is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

It will also serve as a simple adjustable switching regulator, programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the 317T can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2 V where most loads draw little current.

PIN CONNECTIONS

FRONT VIEW





317T

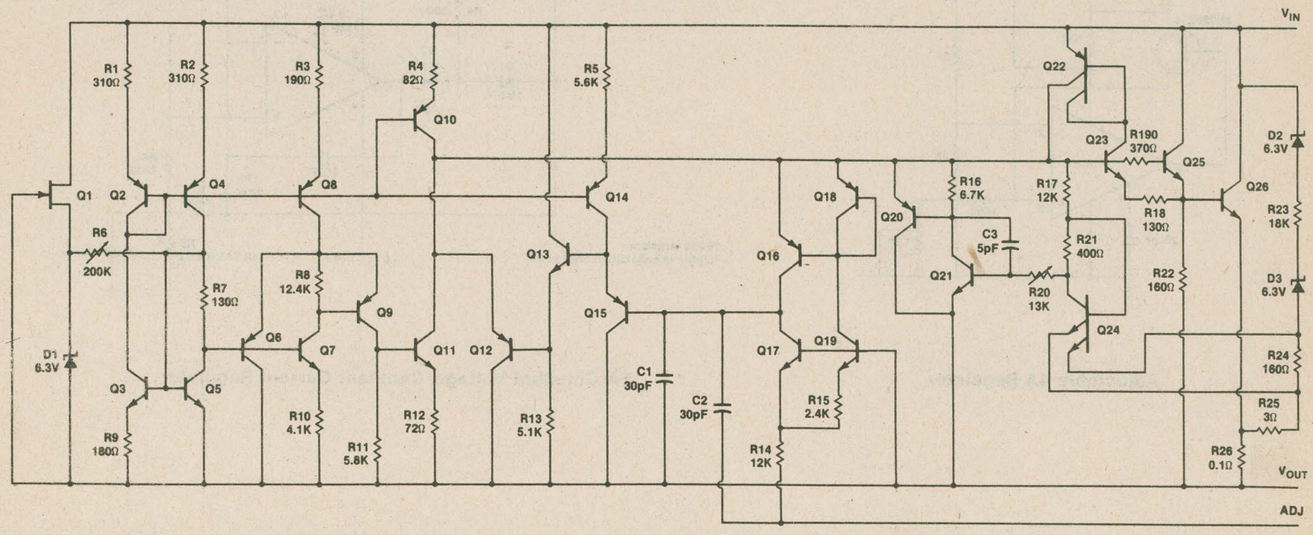
FEATURES

- Adjustable output down to 1.2V
- Guaranteed 1.5A outppput current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

ABSOLUTE MAXIMUM RATINGS

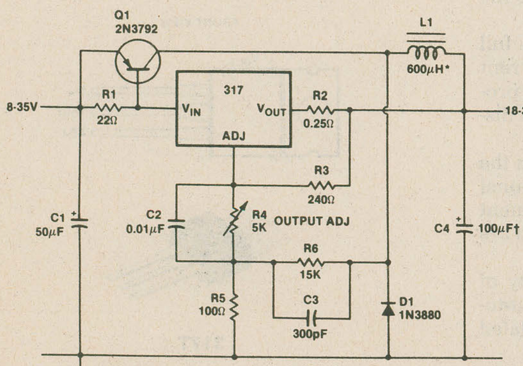
Power Dissipation	Internally limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	0 to +125°C
Storage Temperature	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

INTERNAL CIRCUIT



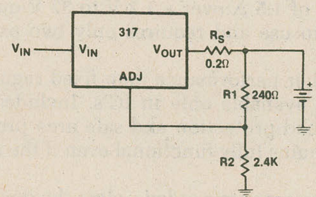
317T 276-1778

TYPICAL APPLICATIONS

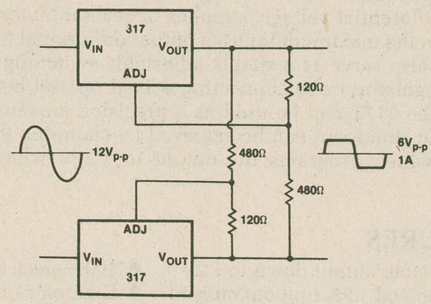


†Solid Tantalum
*Core—Arnold A-254168-2 60 turns

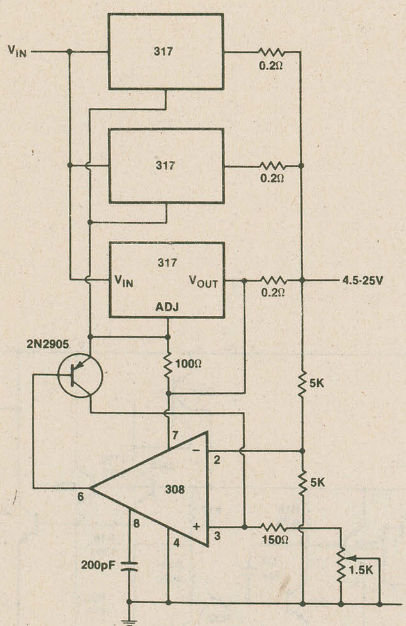
Low Cost 3A Switching Regulator



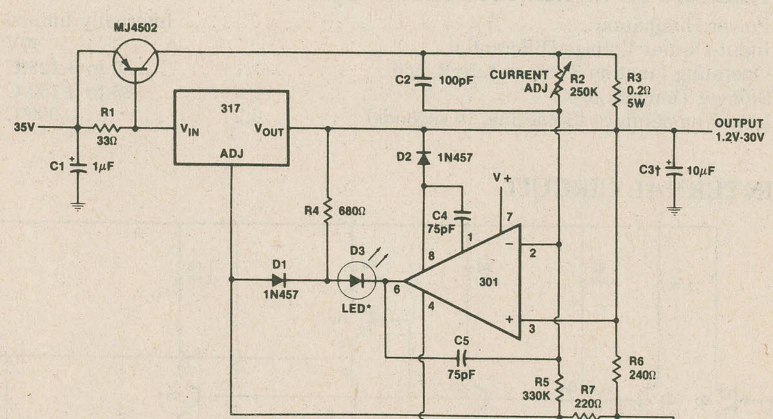
12V Battery Charger



AC Voltage Regulator

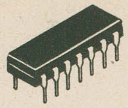


Adjustable 4A Regulator



†Solid tantalum
*Lights in constant current mode

5A Constant Voltage/Constant Current Regulator



ADJUSTABLE VOLTAGE REGULATOR

723
276-1740

GENERAL DESCRIPTION

The 723 is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

FEATURES

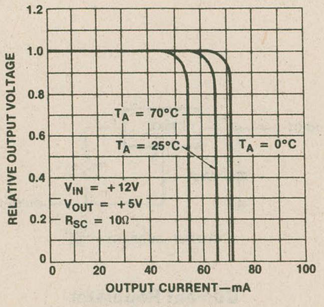
- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

The 723 is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

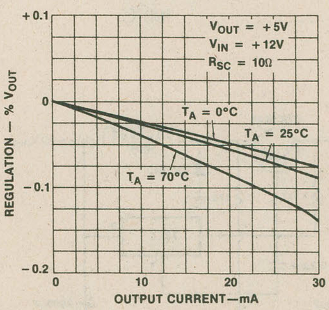
ABSOLUTE MAXIMUM RATINGS

Pulse Voltage from V^+ to V^- (50 ms)	50V
Continuous Voltage from V^+ to V^-	40V
Input-Output Voltage Differential	40V
Maximum Amplifier Input Voltage (Either Input)	7.5V
Maximum Amplifier Input Voltage (Differential)	5V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation Metal Can	800 mW
Cavity DIP	900 mW
Molded DIP	660 mW
Operating Temperature Range	0 to +70°C
Storage Temperature Range Metal Can	−65 to +150°C
DIP	−55 to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

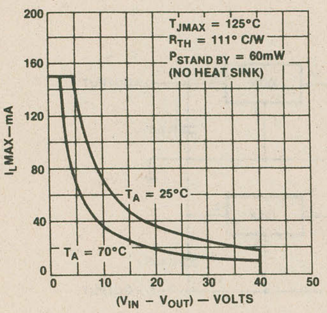
TYPICAL CHARACTERISTICS



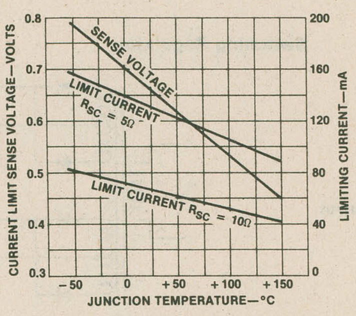
Relative Output Voltage vs Output Current



Load Regulation vs Output Current

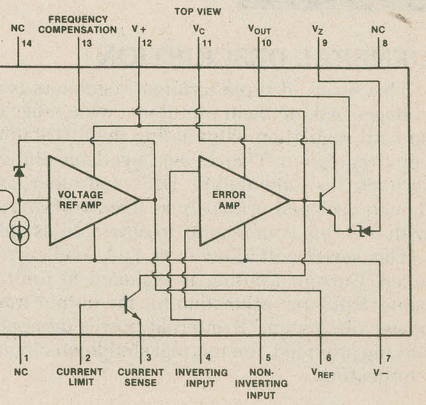


Maximum Load Current vs Input-Output Voltage Differential



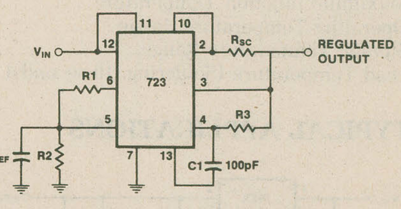
Current Limit Sense Voltage vs Junction Temperature

PIN CONNECTION



TYPICAL APPLICATIONS

(V_{OUT} = 2 to 7 Volts)

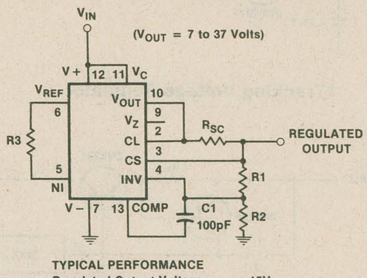


TYPICAL PERFORMANCE

Regulated Output Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 50mA)	1.5mV

Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift.

Basic Low Voltage Regulator



TYPICAL PERFORMANCE

Regulated Output Voltage	15V
Line Regulation (ΔV_{IN} = 3V)	1.5mV
Load Regulation (ΔI_L = 50mA)	4.5mV

Note: $R3 = \frac{R1R2}{R1 + R2}$ for minimum temperature drift.

Basic High Voltage Regulator

7805 276-1770 **7812** 276-1771 **7815** 276-1772

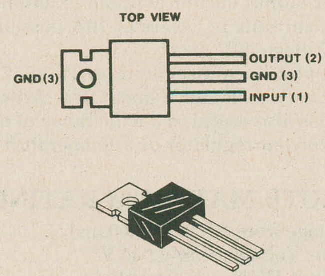
5V VOLTAGE REGULATOR
12V VOLTAGE REGULATOR
15V VOLTAGE REGULATOR

GENERAL DESCRIPTION

This series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

This series will allow over 1.5A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

PIN CONNECTION



FEATURES

- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit

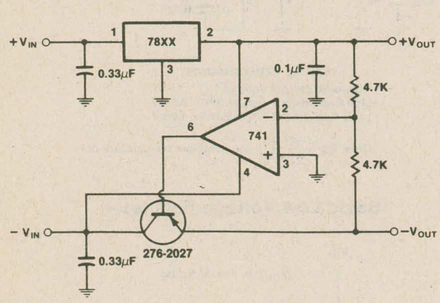
VOLTAGE RANGE

7805 .... 5V
7812 .... 12V
7815 .... 15V

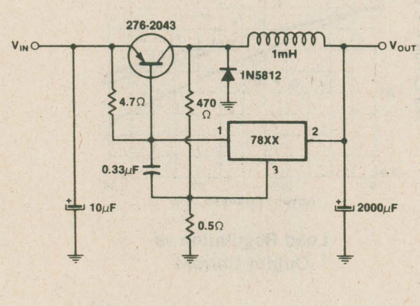
ABSOLUTE MAXIMUM RATINGS

Input Voltage
(Output Voltage Options 5V through 18V) 35V
(Output Voltage Option 24V) 40V
Internal Power Dissipation .... Internally Limited
Maximum Junction Temperature .... 150°C
Operating Temperature Range .... 0 to +70°C
Storage Temperature Range .... −65 to +150°C
Lead Temperature (Soldering, 10 seconds) .... 300°C

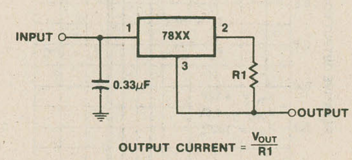
TYPICAL APPLICATIONS



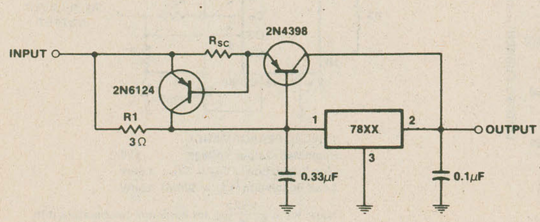
±Tracking Voltage Regulator



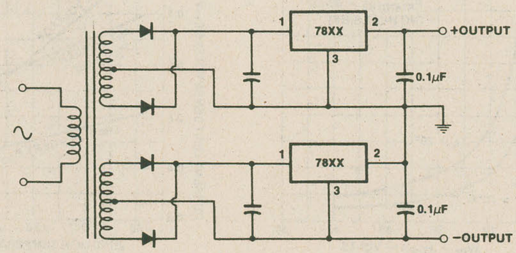
Switching Regulator



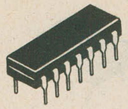
Current Regulator



High Output Current, Short Circuit Protected



Positive and Negative Regulator



QUAD COMPARATOR

339
276-1712

GENERAL DESCRIPTION

The 339 series consists of four independent voltage comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground. even though operated from a single power supply voltage.

FEATURES

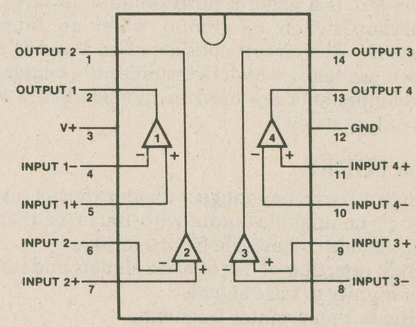
- Wide single supply:
  Voltage range 2 V_{DC} to 32 V_{DC} or dual supplies ±1 V_{DC} to ±16 V_{DC}
- Very low supply current drain (0.8 mA)—independent of supply voltage (1 mW/comparator at +5 V_{DC})
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 1 mV at 5 μA; saturation voltage 70 mV at 1 mA
- Output voltage compatible with TTL (fanout of 2). DTL. ECL. MOS and CMOS logic systems

ABSOLUTE MAXIMUM RATINGS

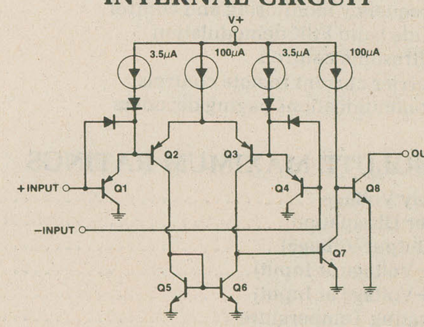
Supply Voltage. V+	32 V_{DC} or ±16 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation	
Molded DIP	570 mW
Cavity DIP	900 mW
Output Short-Circuit to GND	Continuous
Input Current ($V_{IN} < -0.3$ V_{DC})	50 mA
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering. 10 seconds)	300°C

PIN CONNECTION

TOP VIEW

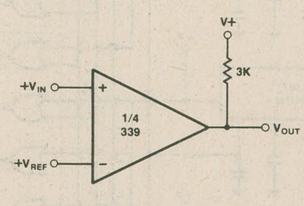


INTERNAL CIRCUIT

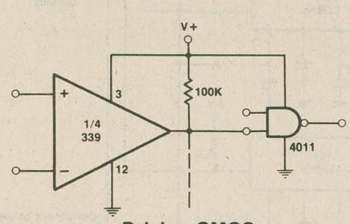


TYPICAL APPLICATIONS

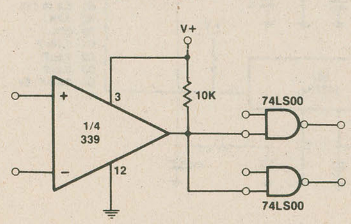
5 VOLT GROUP



Basic Comparator

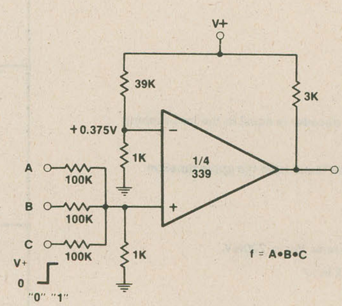


Driving CMOS

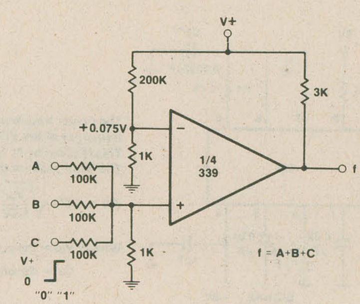


Driving TTL

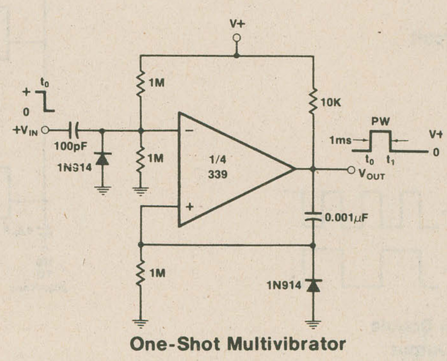
15V GROUP



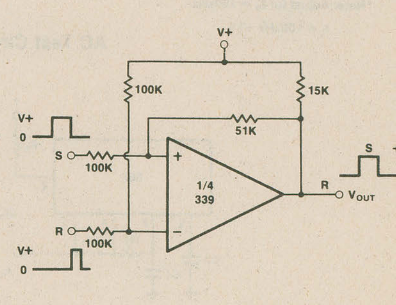
AND Gate



OR Gate



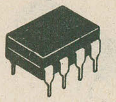
One-Shot Multivibrator



Bi-Stable Multivibrator

567
276-1721

TONE DECODER



GENERAL DESCRIPTION

The 567 is a general purpose tone decoder designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

FEATURES

- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

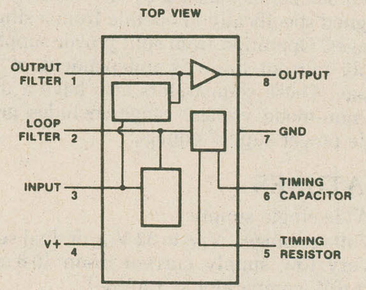
APPLICATIONS

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

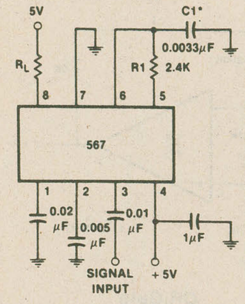
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	9V
Power Dissipation	300 mW
V_8 (Output Voltage)	15V
V_3 (−Voltage at Input)	−10V
V_3 (+Voltage at Input)	V_8+0.5V
Operating Temperature	0 to +70°C
Storage Temperature Range	−65 to +150°C

PIN CONNECTION



TYPICAL APPLICATIONS



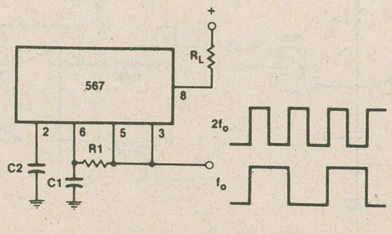
*Note: Adjust for f_o = 100kHz.
f_i = 100kHz +5V

The center frequency of the tone decoder is equal to the free-running frequency of the VCO.
This is given by $f_o \cong 1/R1C1$
The band width of the filter may be found from the approximation

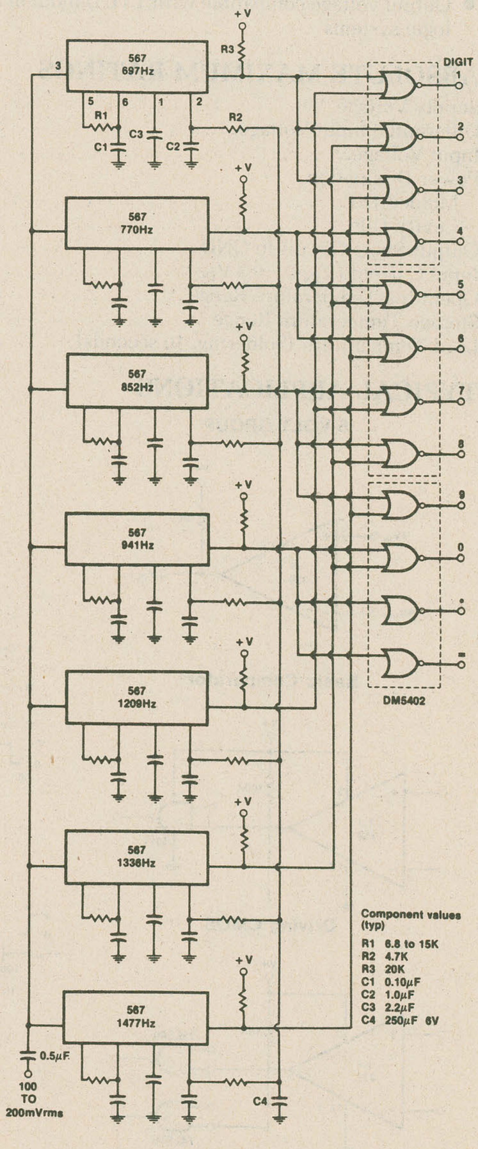
$$BW = 1070\sqrt{\frac{V_{IN}}{f_oC2}} \text{ in \% of } f_o.$$

Where: V_{IN} = Input voltage (volts rms), $V_{IN} \leq$ 200mV.
C2 = Capacitance at pin 2 in μF.

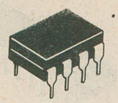
AC Test Circuit



Oscillator with Double Frequency Output



Touch-Tone Decoder



LED FLASHER/OSCILLATOR

3909
276-1705

GENERAL DESCRIPTION

The 3909 is a monolithic oscillator specifically designed to flash light emitting diodes. By using the timing capacitor for voltage boost, it delivers pulses of 2 or more volts to the LED while operating on a supply of 1.5V or less. The circuit is inherently self-starting, and requires addition of only a battery and capacitor to function as a LED flasher.

It has been optimized for low power drain and operation from weak batteries so that continuous operation life exceeds that expected from battery rating.

Application is made simple by inclusion of internal timing resistors and an internal LED current limit resistor.

Timing capacitors will generally be of the electrolytic type, and a small 3V rated part will be suitable for any LED flasher using a supply up to 6V. However, when picking flash rates, it should be remembered that some electrolytics have very broad capacitance tolerances, for example −20% to +100%.

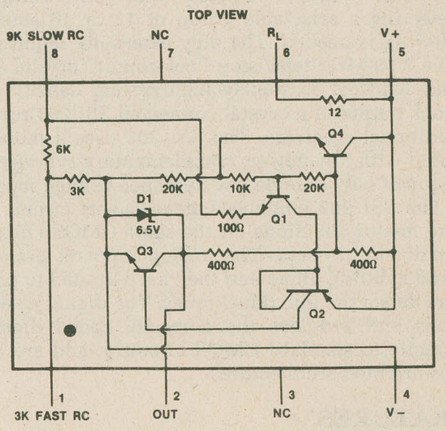
FEATURES

- Operation over one year from one C size flashlight cell
- Bright, high current LED pulse
- Minimum external parts
- Low voltage operation, from just over 1V to 5V
- Low current drain, averages under 0.5 mA during battery life
- Powerful; as an oscillator directly drives an 8Ω speaker

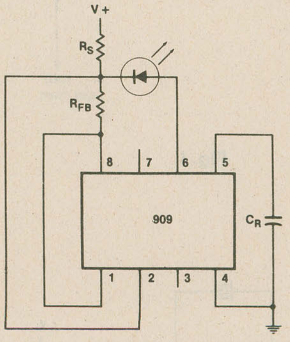
ABSOLUTE MAXIMUM RATINGS

Power Dissipation .... 500 mW
V^+ Voltage 6.4V
Pulse Width .... 6 ms
Peak LED Current .... 45 mA
Operating Current .... 75 mA
Flash Frequency .... 1.3 Hz
High Flash Frequency .... 1.1 kHz
Operating Temperature Range .... −25 to +70°C

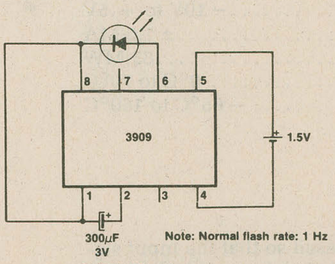
PIN CONNECTION



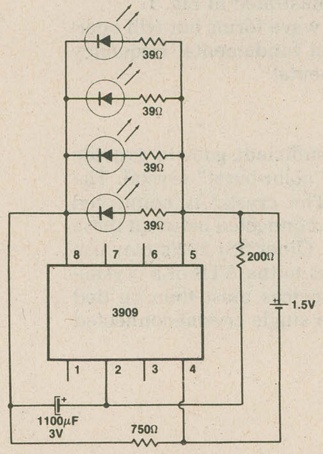
TYPICAL APPLICATIONS



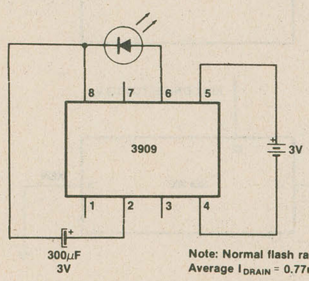
Warning Flasher High Voltage Powered



1.5V Flasher

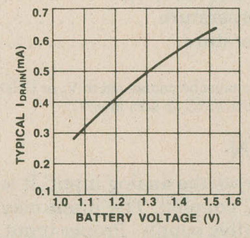


Parallel LED's



3V Flasher

TYPICAL CHARACTERISTICS



Drain Current vs Battery Voltage

ESTIMATED BATTERY LIFE
(CONTINUOUS 1.5V FLASHER OPERATION)

SIZE CELL	TYPE: STANDARD	TYPE: ALKALINE
AA	3 MONTHS	6 MONTHS
C	7 MONTHS	15 MONTHS
D	1.3 YEARS	2.6 YEARS

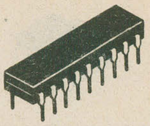
Note: Estimates are made from our tests and manufacturers data. Conditions are fresh batteries and room temperature. Clad or "leak-proof" batteries are recommended for any application of five months or more. Nickel Cadmium cells are not recommended.

TYPICAL OPERATING CONDITIONS

V+	NORMAL FLASH Hz	C_T	R_S 1W	R_{FB}	$V+_{RANGE}$
6V	2	400μF	1K	1.5K	5-25V
15V	2	180μF	3.9K	1K	13-50V
100V	1.7	180μF	43K	1K	85-200V

SSI202
276-1303

5V LOW-POWER DTMF RECEIVER

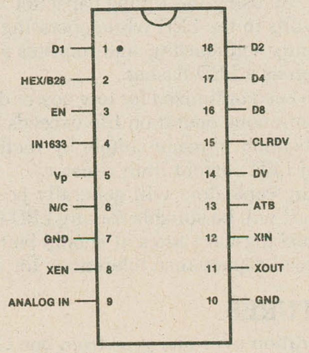


GENERAL DESCRIPTION

The SSI 202 is a complete Dual Tone Multiple Frequency (DTMF) receiver detecting a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.58-MHz television "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is made possible by using the clock output of a crystal connected SSI 202 receiver to drive the time bases of additional receivers. The SSI 202 uses a monolithic integrated circuit fabricated with low-power, complementary symmetry MOS (CMOS) processing. It requires only a single low tolerance voltage supply.

The SSI 202 employs state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is pre-processed by 60-Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

PIN CONNECTION



FEATURES

- NO front-end band-splitting filters required
- Single, low-tolerance, 5-volt supply
- Detects either 12 or 16 standard DTMF digits
- Uses inexpensive 3.579545-MHz crystal for reference
- Excellent speech immunity
- Output in either 4-bit hexadecimal code or binary coded 2 of 8
- Synchronous or handshake interface
- Three-state outputs

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (DC)	7V
Input Voltage (All Inputs Except Analog In)	−.5V to +.5V
Analog In Voltage	−10V to +.5V
DC Current Into Any Input	± 1.0 MA
Power Dissipation (Note 1)	65 MW
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to 150°C

* All unused inputs must be connected to V_p or GND as appropriate.
Note 1: Operate above 25°C @ 6.25 mw/°C

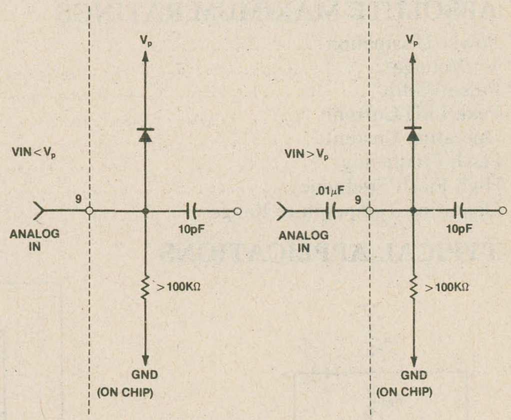


Fig. 1

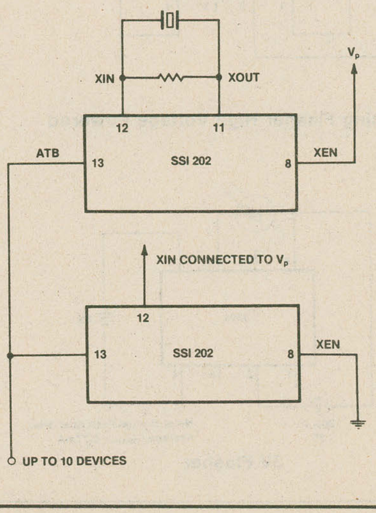
ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Fig. 1.

The SSI 202 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than 20 dB below the fundamental.

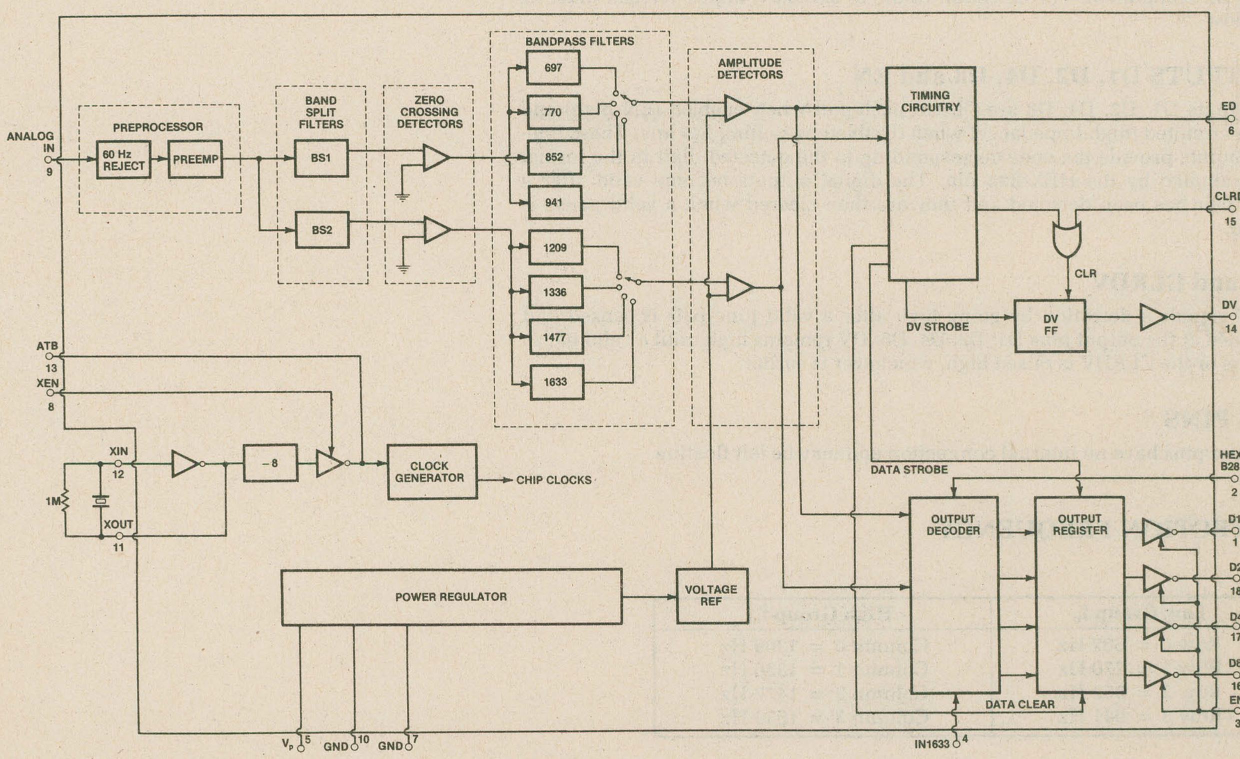
CRYSTAL OSCILLATOR

The SSI 202 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 202's may use the same frequency reference by tying their ATB pins to the ATB of a crystal-connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 202 .



SSI202 276-1303

Block Diagram



HEX/B28

This pin selects the format of the digital output code. When HEX/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2 of 8. The table below describes the two output codes.

	Hexadecimal				Binary Coded 2 of 8			
Digit	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

SSI202 276-1303

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633-Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the HEX/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever is earlier.

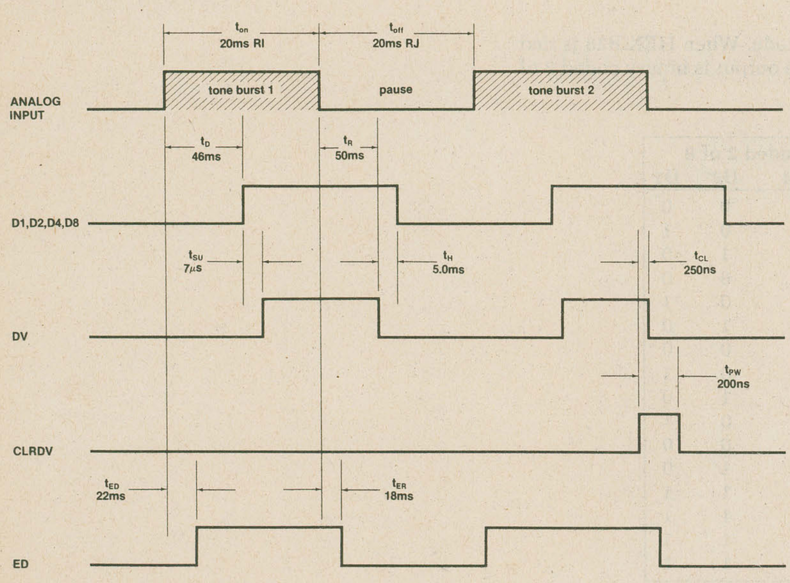
N/C PINS

These pins have no internal connection and may be left floating.

DETECTION FREQUENCY

Low Group f_o	High Group f_o
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

SSI 202 TIMING



CODE-TO-SPEECH CHIP

CTS256AL2
276-1786

GENERAL DESCRIPTION

The Code-To-Speech chip set consists of two chips: the SPO256A-AL2, an allophone-base single chip speech synthesizer, and the CTS265A-AL2, an 8-bit microcomputer programmed with a letter-to-sound based algorithm. This chip set translates English characters into LPC synthesized speech sounds.

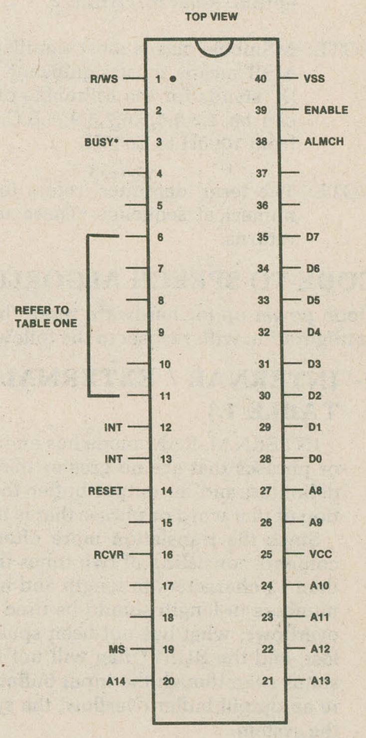
The SPO256A-AL2 is a standard allophone chip and is based on the SPO256A speech synthesizer. This synthesizer consists of a 10 or 12 pole second-order cascaded LPC filter, a controller, and a 16-Kbit ROM in which 59 allophones (speech sounds) and five pauses are stored.

The CTS256A-AL2 is a device whose on-board ROM is masked with code-to-speech algorithm. This algorithm converts English text (in the form of standard ASCII characters) into SPO256A-AL2 compatible allophone addresses, using letter-to-sound rules.

This chip set delivers highly recognizable speech output from any peripheral device or computer in a flexible and cost effective manner. It can be configured as a dedicated code-to-speech system, as well as add speech output to a user's program running in this CTS256A-AL2 from off-chip Rom. Such user programs are written in PIC7001 assembly language which is 100% compatible with TMS7001 assembly language.

Eproms can be added to improve the pronunciation of certain proper names, acronyms and technical words as well as to store user programs.

PIN CONNECTION



FEATURES:

- Unlimited vocabulary
- Utilizes letter-to-sound rules
- Serial or parallel interface
- Microprocessor available for user code

PIN SELECTABLE CODE-TO-SPEECH OPTIONS:

Refer to TABLE 1.

INPUT INTERFACE	—Serial port & baud rate vs. Parallel port
INPUT BUFFER	—Internal RAM vs. External RAM
DELIMITER	—Any-delimeter vs Carriage-return-only
UART PARAMETERS	—Program defaults vs 74LS373 selectable (or eprom definable)

FIRMWARE (EXCEPTION-WORD/USER EPROM) CONTROLLED CODE-TO-SPEECH OPTIONS: (optional)

Refer to TABLE 2.

- Parallel port decode relocatable
- UART parameters 74LS373 decode relocatable
- UART parameters selectable
- Start & end address of External-Ram relocatable

CODE-TO-SPEECH ALGORITHM FEATURES:

-ESCAPE	"ESC", (1B Hex)	THE ESCAPE-KEY CODE WILL DUMP THE CONTENTS OF THE INPUT AND OUTPUT BUFFERS, AND WILL ALSO SILENCE SPEECH OUTPUT WHICH IS IN PROGRESS.
-BACKSPACE	"<-", (0B Hex)	THE BACKSPACE-KEY CODE ERASES THE INPUT BUFFER ONE CHARACTER AT A TIME, BEGINNING WITH THE LATEST ENTRY.

NOTE: The R/C combination indirectly connected to PIN 14 of the CTS256A-AL2 and to PIN 2, 25 of the SPO256A-AL2 acts as a power-on reset. The requirement to reset the chip-set is a negative-going pulse which remains LO for a minimum of 500 microseconds.

NOTE: A signal (input or output) that is active-LO is designated by its signal name followed by an asterisk (*).

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CODE-TO-SPEECH ALGORITHM (Cont'd)

NOTE: The program default address decode of the SPO256A-AL2's ALD* input is 2000H. It is re-definable via the EXCEPTION-WORD or USER eprom. Refer to TABLE 2. 8k

NOTE: MSnibble means most significant nibble, where a nibble is half a byte. MSB means most significant byte; LSB means least significant byte. 'X' stands for the MSnibble of the MSB of the two byte address, and can be 1,2,3,4,5,6,7,8,9,A,B,C,D, or E because an eprom may reside from 1000H to E000H.
4K 56K

NOTE: The term 'delimiter' refers to any punctuation following a word or numerical sequence. These include: , . ; : ! ? spaces and carriage-returns.

CODE-TO-SPEECH ALGORITHM

Upon power-up (or hardware reset) the CTS256A-AL2 determines the system configuration with respect to the following five options:

1- INTERNAL / EXTERNAL RAM SELECTION: (Refer to TABLE 1.)

INTERNAL-RAM mode has an input buffer which accommodates words or phrases that are no greater than 19 characters in length followed by a delimiter; and an output buffer that accommodates an allophone translation of that word or phrase that is no greater than 26 allophone addresses.

Since the translation more often than not results in the output buffer contents consisting of two times that of the input buffer, words no longer than 13 characters in length and numerical sequences of no longer than 4 numbers in length should be used as a rule of thumb. If the output buffer overflows, what has not been spoken yet from the output buffer might be lost, and the BUSY* flag will not necessarily show an input buffer empty status even though the input buffer might be empty. If a translation results in an output buffer overflow, the system reset may have to be used to clear the system.

EXTERNAL-RAM mode can be used to extend the size of the input and output buffers. If no EXCEPTION-WORD or USER eproms are present, the start address default is 3000H. Static RAM can be added in 256 byte contiguous block increments, beginning with a minimum of 512 bytes. The algorithm will find the end address by searching for the first non-RAM location at 256 byte intervals. The search for the end address will not progress beyond 2K bytes. 12 K

start of RAM 12K
end " " 14 2K

If an eprom is present, the start and end addresses are re-definable there. Requirements are: minimum start address is 0200H; the start address must begin on a boundary where the LSByte of the address =00; and without the end address specified in eprom, the maximum valid start address is EE00H. 59.5K 512

In any case, 256 bytes are taken for the output buffer; the remainder is the input buffer. (External-Ram used must have an access time of 250 nS or less.)

2- ROM:

4K 56K

A search is made from 1000H to E000H is 4K increments for the 5 byte sequence (80H, 48H, 28H, 58H, 85H) which uniquely identifies the presence of an EXCEPTION-WORD or USER eprom. If neither are present, the system options are set to algorithm default values or can be chosen by the Pin selectable options. If only a USER eprom is present, the system options may be re-defined from the USER eprom; refer to APPENDIX-0. If both USER and EXCEPTION-WORD eproms are present or if only an EXCEPTION-WORD eprom is present, the system option may be re-defined from the EXCEPTION-WORD eprom; refer to APPENDIX-A,B. (External-Ram used must have an access time of 300nS or less.)

Exception-Word Eprom(s): (optional)

Exception-word eprom(s) say reside anywhere within the decodeable addresspace of the CTS256A-AL2 from 1000H 4K to E000H, 56K providing its start address falls on a 4K boundary. The code-to-speech initialization routine will search for its existence which is denoted by a unique 5-byte sequence of numbers (80H, 48H, 28H, 58H, 85H). A few other locations in the primary
128 72 40 88 133

Exception-Word Eprom(s): (Cont'd)

exception-word eprom are reserved, and must contain specific sequences of numbers; the remainder are user-defined. Additional exception-word eprom(s) contiguous to the primary exception-word eprom contain no reserved locations. Refer to APPENDIX-A, B for the applicable EXCEPTION-WORD EPROM MEMORY MAP.

User-Eprom(s): (optional)

If a USER eprom is accompanied by an EXCEPTION-WORD eprom, it may reside anywhere. If no EXCEPTION-WORD eprom accompanies it then it may reside anywhere from 1000H to E000H providing its start address falls on a 4K boundary; and it must then begin with the sequence 80H, 48H, 28H, 58H, 85H; and also contain other reserved locations. If an EXCEPTION-WORD eprom is present, the USER's program can even reside in an unused portion of the EXCEPTION-WORD eprom. Refer to APPENDIX-D,E for the applicable USER EPROM MEMORY MAP.

Interaction between a USER program and the code-to-speech algorithm must be controlled in an orderly manner, ie; the user must save the processor status before taking control of the processor for execution of any USER code (except for character string loading operations, which is described next:)

To prepare the code-to-speech algorithm to process and speak, the USER program passes the character string it wants spoken into the Accumulator one character at a time, then calls the routine @SAVE which transfers it into the input buffer. After the character string loading has been completed, the USER code can initiate the speech by calling the @SPEAK routine; assuming that a delimiter followed that character string. After the loaded character string is processed and spoken, program control resumes in the hands of the USER program by the Branch @USERCODE instruction.

No registers used by the code-to-speech algorithm may be disturbed by the USER code during character string loading, (except for the Accumulator).

Prior to the USER code executing anything other than character string loading, all registers used by the code-to-speech algorithm as well as the Stack Pointer and STATUS register are to be saved. These registers must be recovered prior to future character string loading operations; or prior to initiating speech.

Because of masked code-to-speech restrictions within the CTS256A-AL2, Interrupt-1* and Interrupt-3* are not USER accessible. Also, input from the serial port into the USER code can be obtained, but restrictions apply.

Refer to APPENDIX-F for a discussion of the sequence of events and subroutines necessary for USER/CODE-TO-SPEECH interactions as described above.

3- Serial / Parallel Input Interface Selection: (Refer to TABLE 1.)

In the parallel mode, ASCII data is latched by an 74LS374, upon receipt of an Active LO data-valid strobe. This strobe also vectors the algorithm to accept the data via Interrupt-3*, PIN 12 of the CTS256A-AL2. The latch's address default is 200H. It is re-definable from EXCEPTION-WORD or USER eprom. (Refer to TABLE 9 for timing requirements of the parallel port.)

In the serial mode, ASCII data is accepted via the CTS256A-AL2 PIN 16, which is a built-in UART that requires a TTL level signal input. The baud rate is selectable at 50,110,300,1200,2400,4800 and 9600. The other UART parameters are set to algorithm default values, or are hardware selectable via an 74LS373 buffer. The buffer address default is 1000H. The UART parameters as well as the baud rate is re-definable from EXCEPTION-WORD or USER eprom. The algorithm default UART values are: Asynchronous, 7 bits/character, 2 stop bits, and no parity.

In either serial or parallel mode, the input buffer is protected from overflow by a hysteresis subroutine which signals the host when the input buffer is full, and when the input buffer is ready for additional input. Hardware handshaking (BUSY*) is provided to accomplish this signaling of input buffer status.

BUSY* is Active-LO. It toggles LO when the input buffer becomes 87.5% full. In this way the host system may use its discretion to complete that transmission or a part thereof. If the input buffer becomes 100% full, the parallel and serial port interrupts are disabled to prevent input buffer overwrite; and the interrupts are not re-enabled until the input buffer full condition has dissipated. BUSY* will toggle hi when the input buffer becomes 50% empty; at which time the interrupts are enabled if they had been disabled by a 100% full condition. (BUSY* is PIN-3 of the CTS256A-AL2 which is a TTL level output capable of sinking 10 mA maximum.)

CTS256AL2 276-1786

4- Software / Hardware (or Firmware) UART Parameters Selection: (Refer to TABLE 1.)

This hardware option tells the code-to-speech algorithm to use the default UART values, or to find the parameters at the 74LS373 buffer. The buffer address default is 1000H. The UART parameters are re-definable from eprom, but only if the hardware mode is selected via Pin 9 of the CTS256A-AL2.

4K

5- Any-Delimiter / Carriage-Return-Only Selection: (Refer to TABLE 1.)

In the any-delimiter mode, the code-to-speech algorithm will process and speak words or phrases as soon as they are followed by any delimiter. In the carriage-return-only mode, the algorithm will process and speak words or phrases only after a carriage-return is received as a delimiter. The carriage-return-only mode is meant for use with a slow input device such as a terminal, where the user wishes to buffer-up a complete phrase so that it is spoken with fluency. If the carriage-return-only mode is chosen in conjunction with EXTERNAL-RAM, limit to 160 characters the length of the phrase which is entered before the carriage-return is entered. This allows for a two line phrase to be spoken with fluency while insuring that the 256 byte output buffer should not overflow.

After completion of the initialization the phrase "O.K." is spoken to demonstrate that the system is ready for input, then one of the following two paths is taken dependent upon the system configuration:

1: In a 'dedicated code-to-speech system' (ie; USER eprom is not present), the algorithm idles as long as the input buffer remains empty. Input is via standard ASCII characters. Processing begins with an alphabetical search of the EXCEPTION-WORD eprom, if it is present. If no exact match for the character string is found, or if an EXCEPTION-WORD eprom is not present, the algorithm employs a letter-to-sound rule table against which main, right, and left context matches are performed. This results in the translation of a particular word into the proper string of allophone addresses necessary for its pronunciation. This list of allophone address is sent to the SP0256A-AL2 after a carriage-return, or after any delimiter—depending on the mode selected.

2: In the 'add speech to USER's program' mode (ie; USER eprom is present), control of the processor is relinquished to the USER code immediately after the initialization is complete. The USER code may then execute its own code, may pass character strings into the input buffer memory, or may hand-off processor control to the code-to-speech algorithm to speak any previously loaded character strings. If speech is initiated, control returns to the USER code after the last delimited character string in the input buffer has been processed. Refer to APPENDIX-F.

TABLE 1.

Hardware selectable option pin-outs of CTS256A-AL2:

PIN 6	7	8		
0	0	0	←PARALLEL INPUT MODE	
0	0	1	BAUD 50	SERIAL INPUT MODE
0	1	0	BAUD 110	SERIAL INPUT MODE
0	1	1	BAUD 300	SERIAL INPUT MODE
1	0	0	BAUD 1200	SERIAL INPUT MODE
1	0	1	BAUD 2400	SERIAL INPUT MODE
1	1	0	BAUD 4800	SERIAL INPUT MODE
1	1	1	BAUD 9600	SERIAL INPUT MODE

PIN 9

- 0 ←PROGRAM DEFAULT UART VALUES (Asynchronous, 7 bits/character, 2 stop bits, no parity).
- 1 ←HARDWARE (or FIRMWARE) SELECTED UART VALUES.

PIN 10

- 0← INTERNAL-RAM BUFFERS, (20 BYTE INPUT/26 BYTE OUTPUT).
- 1← EXTERNAL-RAM BUFFERS, (1792 BYTE INPUT/256 BYTE OUTPUT WITH A 2-KBYTE RAM).

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TABLE 1. Con't.

PIN 11
- 0 ← CARRIAGE-RETURN-ONLY DELIMITER.
- 1 ← ANY DELIMITER.

PIN 03 "BUSY$" (Input buffer flag is a TTL level output); for RS232 compatibility use MC1488 Line Driver or equiv.
- 0 → INPUT BUFFER IS > = 87.5% FULL.
- 1 → INPUT BUFFER IS < = 50.0% EMPTY.

PIN 16 → UART RECEIVER (Serial input is a TTL level input); for RS232 compatibility use MC1489 Line Receiver or equiv.

NOTE: 0 implies TLL LO level; 1 implies TTL HI level.
← implies input; → implies output.

A typical connection to a computer with an RS232 interface:

COMPUTER		CODE-TO-SPEECH CHIP-SET
protective GND	↔	signal GND (Circuit ground).
signal GND	↔	signal GND (Circuit ground).
Clear To Send (CTS)	←	Request To Send (RTS) = CTS256A-ALs's PIN 3 (BUSY$).
Transmitter's Line Driver	→	CTS256A-AL2 UART's Line Receiver.

TABLE 2. NEW PARAMETERS.

X009	FF	NUMBER OF BYTES OF 50% OF EXTERNAL INPUT BUFFER (MSB)	4105
X00A	FF	NUMBER OF BYTES OF 50% OF EXTERNAL INPUT BUFFER (LSB)	4106
X00B	FF	NUMBER OF BYTES OF 12.5% OF EXTERNAL INPUT BUFFER (MSB)	4107
X00C	FF	NUMBER OF BYTES OF 12.5% OF EXTERNAL INPUT BUFFER (LSB)	4108
X00D	FF	EXTERNAL RAM START ADDRESS (MSB) see note 2.3	4109
X00E	FF	EXTERNAL RAM START ADDRESS (LSB) see note 2.3	4110
X00F	FF	EXTERNAL RAM END ADDRESS-100H (MSB) see note 2.3	4111
X010	FF	EXTERNAL RAM END ADDRESS-100H (LSB) see note 2.3	4112
X011	FF	EXTERNAL RAM START ADDRESS-1 (MSB) see note 2.3	4113
X012	FF	EXTERNAL RAM START ADDRESS-1 ~~(LSB) see note~~ 2.3	4114
X013	FF	EXTERNAL RAM END ADDRESS-FFH (MSB) see note 2.3	4115
X014	FF	EXTERNAL RAM END ADDRESS-FFH (LSB) see note 2.3	4116
X015	FF	EXTERNAL RAM END ADDRESS + 1 (MSB) see note 2.3	4117
X016	FF	EXTERNAL RAM END ADDRESS + 1 (LSB) see note 2.3	4118
X017	FF	ADDRESS DECODE OF SPO256A-AL2's ALD$ (MSB) see note 2.4 Address of speech chip.	4119
X018	FF	ADDRESS DECODE OF SPO256A-AL2's ALD$ (LSB) see note 2.4	4120
X019	FF	ADDRESS DECODE OF 74LS374 PARALLEL PORT LATCH (MSB)	4121
X01A	FF	ADDRESS DECODE OF 74LS374 PARALLEL PORT LATCH (LSB)	4122
X01B	FF	see note 2.1	4123
X01C	FF	TOTAL NUMBER OF BYTES IN INPUT BUFFER (MSB)	4124
X01D	FF	TOTAL NUMBER OF BYTES IN INPUT BUFFER (LSB)	4125
X01E	FF	see note 2.1	4126
X01F	FF	see note 2.1	4127
X020	FF	SERIAL PORT REGISTER (see table 5) see note 2.5	4128
X021	FF	SERIAL PORT CONTROL REGISTER (see table 6) see note 2.5 see Table #5	4129
X022	FF	SERIAL PORT TIMER DATA REGISTER (see table 6) see note 2.5	4130

YOUR EXCEPTION-WORD OR USER EPROM CAN RESIDE ANYWHERE FROM 1000H TO E000H PROVIDING IT BEGINS ON A 4K BOUNDARY WHERE X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E. (The least significant 3 nibbles of the address must remain as shown.)

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NOTE 2.1 THESE LOCATIONS MUST BE FF, (THEY ARE NOT USER DEFINABLE).
NOTE 2.2 TO MAINTAIN ANY PARAMETER AT ITS DEFAULT VALUE, LOAD THAT LOCATION WITH FFH.
NOTE 2.3 IF ANY OF THE EXTERNAL RAM BUFFER PARAMETERS ARE REDEFINED HERE, ALL OF THEM MUST BE REDEFINED HERE.
NOTE 2.4 NO MATTER WHAT ADDRESS IS CHOSEN FOR ALD$, THAT ADDRESS THRU THAT ADDRESS + 3FH IS RESERVED FOR SPO256A-AL2 ADDRESSING.
NOTE 2.5 IF ANY OF THE SERIAL PORT PARAMETERS ARE REDEFINED HERE, ALL OF THEM MUST BE REDEFINED HERE.
NOTE 2.6 H, AS IN 100H REFERS TO HEXADECIMAL NOTATION.
NOTE 2.7 A NIBBLE IS HALF OF A BYTE, OR 4 BITS.

TABLE 3. SAMPLE OF ASSEMBLED ALPHABETIZED EXCEPTION-WORD INDEX.

X0A3	X1	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "A"
X0A4	93	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "A"
X0A5	X1	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "B"
X0A6	A8	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "B"
X0A7	X1	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "C"
X0A8	A9	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "C"
X0A9	X1	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "D"
X0AA	B1	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "D"
X0AB	X1	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "E"
X0AC	B2	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "E"
X0AD	X1	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "F"
X0AE	B3	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "F"
X0AF	X1	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "G"
X0B0	B4	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "G"
X0B1	X1	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "H"
X0B2	E1	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "H"
X0B3	X1	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "I"
X0B4	E2	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "I"
X0B5	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "J"
X0B6	OD	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "J"
X0B7	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "K"
X0B8	OE	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "K"
X0B9	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "L"
X0BA	OF	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "L"
X0BB	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "M"

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TABLE 3. (Cont'd)

X0BC	1B	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "M"
X0BD	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "N"
X0BE	1C	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "N"
X0BF	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "O"
X0CO	1D	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "O"
X0C1	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "P"
X0C2	1E	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "P"
X0C3	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "Q"
X0C4	2D	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "Q"
X0C5	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "R"
X0C6	2E	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "R"
X0C7	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "S"
X0C8	2F	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "S"
X0C9	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "T"
X0CA	3O	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "T"
X0CB	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "U"
X0CC	3D	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "U"
X0CD	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "V"
X0CE	5A	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "V"
X0CF	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "W"
X0DO	5B	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "W"
X0D1	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "X"
X0D2	64	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "X"
X0D3	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "Y"
X0D4	65	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "Y"
X0D5	X2	MSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "Z"
X0D6	6F	LSB OF POINTER TO START OF EXCEPTION-WORD BEGINNING WITH "Z"
X0D7	X2	MSB OF POINTER TO START EXCEPTION-WORD BEGINNING WITH "NUMBER OF PUNCTUATION"
X0D8	7O	LSB OF POINTER TO START EXCEPTION-WORD BEGINNING WITH "NUMBER OF PUNCTUATION"

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The least significant nibble of the MSB and the entire LSB address locations will vary with a different set of exception words; X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E.

YOUR EXCEPTION-WORD EPROM CAN RESIDE ANYWHERE FROM 1000H TO E000H PROVIDING IT BEGINS ON A 4K BOUNDARY WHERE X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E. (The least significant 3 nibbles of the address must remain as shown.)

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TABLE 4. SAMPLE OF ASSEMBLED ENCODED EXCEPTION-WORDS

```
A  X193 13 6E 24 AA:DB 19,110,36,185,19,90,11,1,33,19,0,18,15,0,1,65,34,39,20,141
   X196 B9 13 5A 0B 01 21 13 00 12 0F
   X1A0 00 01 41 22 27 14 8D
                    ;<[ANDY]< = [AE NN1 PA2 DD2 IY PA1 DH1 AX PA1 PA2 GG3 RR2 EY TT2] ANDY-THE-GREAT
   X1A7 FF             DB 255
                    ;
B  X1A8 FF          BB:DB 255
                    ;
C  X1A9 13 61 B0    C:  DB 19,97,176,33,106,20,137;<[CAP]A = [KK1 EY PP]          CAPABILITY
   X1AC 21 6A 14 89
   X1B0 FF             DB 255
                    ;
D  X1B1 FF          D:  DB 255
                    ;
E  X1B2 FF          E:  DB 255
                    ;
F  X1B3 FF          F:  DB 255
                    ;
G  X1B4 13 E9 13 6: DB 19,233,19,74,7,11,51,62,0,12,11,55,13,39,31,16,7,11,2,141
   X1B7 4A 07 0B 33 3E 00 0C 0B 37 0D
   X1C1 27 1F 10 07 0B 02 BD
                    ;<[GI]< = [JH EH NN1 ER1 EL PA1 IM NN1 SS TT2 RR2 UW2 MM EH NN1 PA3 TT2]
                    ;GENERAL INSTRUMENT
   X1C8 13 E9 2D       DB 19,233,45,33,41,44,19,74,7,11,51,62,0,12,11,55,13,39,31,16,7,11,2,141
   X1CB 21 29 2C 13 4A 07 0B 33 3E 00
   X1D5 0C 0B 37 0D 27 1F 10 07 0B 02
   X1DF 8D
                    ;<[GI][MAIL< = [JH EH NN1 ER1 EL PA1 IH NN1 SS TT2 RR2 UW2 MM EH NN1 PA3 TT2]
   X1E0 FF             DB 255
                    ;
H  X1E1 FF          H:  DB 255
                    ;
I  X1E2 13 E4 13    I:  DB 19,228,19,70,0,33,7,11,2,13,12,40,12,2,42,20,37,15,139;<[ID]< = [AY PA1
   X1E5 46 00 21 07 0B 02 0D 0C 2B 0C
   X1EF 02 2A 14 25 0F 8B
                    ;DD2 EH NN1 PA3 TT2 IH FF IH PA3 KK1 EY SH AX NN1)          IDENTIFICATION
   X1F5 13 73 2C       DB 19,115,44,165,19,70,1,190;<[ISLE]< = [AY PA2 EL]      ISLE
   X1FB A5 13 46 01 BE
   X1FD 13 73 2C       DB 19,115,44,33,46,164,19,70,0,45,26,11,1,21,1;<[ISLAND]< = [AYPA2ELAENN1DD1]
   X200 21 2E A4 13 46 00 2D 1A 0B 01
   X20A 15 01
   X20C FF             DB 255
                    ;
J  X20D FF          J:  DB 255
                    ;
K  X20E FF          K:  DB 255
                    ;
L  X20F 13 69 36    L:  DB 19,105,54,37,164,19,109,12,35,3,149;<[LIVED]< = [LL IH VV PA4 DD1]          LIVED
   X212 25 A4 13 6D 0C 23 03 95
   X21A FF             DB 255
                    ;
M  X21B FF          M:  DB 255
                    ;
N  X21C FF          N:  DB 255
                    ;
O  X21D FF          O:  DB 255
                    ;
P  X21E 13 75 32    P:  DB 19,117,50,48,47,51,165,19,73,51,9,15,55,183;<[PURPOSE]< = [PPER1PPAXSSSS]
   X221 30 2F 33 A5 13 49 33 09 0F 37
   X22B B7
   X22C FF             DB 255
                    ;
Q  X22D FF          Q:  DB 255
                    ;
R  X22E FF          R:  DB 255
                    ;
S  X22F FF          S:  DB 255
                    ;
```

TABLE 4. (Cont'd)

```
X230 13 6F 34    T: DB 19,111,52,33,172,19,77,53,13,0,15,190;<[TOTAL]< =[TT2 OW TT1 PA1 AX EL]
X233 21 AC 13 4D 35 0D 00 0F BE
X23C FF             DB 255
                 ;
X23D 13 73 25    U: DB 19,115,37,50,41,164,19,113,22,43,51,1,6,0,33,7,11,2,13,12,40,12,2,42,20,37
X240 32 29 A4 13 71 16 2B 33 01 06
X24A 00 21 07 0B 02 0D 0C 2B 0C 02
X254 2A 14 25
X257 0F BB          DB 15,139;<[USERID]< =[YY1 UM1 ZZ ER1 PA1 AY PA1 DD2 EH NN1 PA3 TT2 IH FF IH
                           ;PA3 KK1 EY SH AX NN1]
X259 FF             DB 255
                 ;
X25A FF          V: DB 255
                 ;
X25B 13 65 07    W: DB 19,101,7,50,165,110,19,180                  ;<[WE'RE]=[WW IY ER2]          WE'RE
X25E 32 A5 6E 13 B4
X263 FF             DB 255
X264 FF          X: DB 255
                 ;
X265 13 6F 35    Y: DB 19,111,53,7,50,165,19,89,186        ;<[YOU'RE]< =[YY2 0R]                  YOU'RE
X268 07 32 A5 13 59 BA
X26E FF             DB 255
                 ;
X26F FF          Z: DB 255
                 ;
X270 13 CF 13    NUMORPUN: DB 19,207,19,89,58,1,16,7,55,55,12,1,10,0,2,42,26
X273 59 3A 01 10 07 37 37 0C 01 0A
X27D 00 02 2A 1A
X281 0B 01 3F       DB 11,1,63,19,0,55,55,2,9,53,2,42,7,11,0,46,12,29,0,18,15,0,2,13,15,2,50
X284 13 00 37 37 02 09 35 02 2A 07
X2BE 0B 00 2E 0C 1D 00 12 0F 00 02
X29B 0D 0F 02 32
X29C 00 0F 23       DB 0,15,35,0,20,0,2,42,19,128
X29F 00 14 00 02 2A 13 80
                 ;<[/]< =[YY1 OR PA2 MM EH SS SS IH PA2 JH PA1 PA3 KK1 AE NN1 PA1 PA2 BB2 IY
                 ;PAI SS SS PA3 PP OW PA3 KK1 EM NN1 PA1 WW IH TH PA1 DH1 AX PA1 PA3
                 ;TT2 AX PA3 CH PA1 AX VV PA1 EY PA1 PA2 KK1 EY PA1]YOU'RE MESSAGE CAN BE SPOKEN
                 ;WITH THE TOUCH OF A KEY
                 ;
X2A6 C6 5A 0B       DB 198,90,11,21,128            ;[&]=[AE NN1 DD1 PA1]                   AND
X2A9 15 80
X2AB FF             DB 255                         ;MUST END EACH CATEGORY WITH [  ].
↑
└──WHERE X=1,2,3,4,5,6,7,8,9,A,B,C,D, or E. (The least significant 3 nibbles of the address
   will vary with a different set of exception words.)
```

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TABLE 5. SERIAL PORT MODE REGISTER

MSB 7	6	5	4	3	2	1	LSB 0
STOP	SIO	PEVEN	PEN	CHAR1	CHAR0	COMM	MULTI

MULTI:
0 = MOTOROLA PROTOCOL
1 = INTEL PROTOCOL

COMM:
0 = ISOSYNCHRONOUS COMMUNICATION
1 = ASYNCHRONOUS COMMUNICATION

CHAR1, CHAR0:
00 = 5 BITS/CHARACTER
01 = 6 BITS/CHARACTER
10 = 7 BITS/CHARACTER
11 = 8 BITS/CHARACTER

PEN:
1 = PARITY ENABLED
0 = PARITY DISABLED

PEVEN:
1 = EVEN PARITY
0 = ODD PARITY

SIO:
0 = SERIAL I/O MODE
1 = COMMUNICATION MODE

STOP:
0 = ONE STOP BIT
1 = TWO STOP BITS

FOR TYPICAL APPLICATIONS USE: MOTOROLA PROTOCOL, ASYNCHRONOUS COMMUNICATION, 7 BITS/CHARACTER, and COMMUNICATION MODE; THE NUMBER OF STOP BITS AND PARITY MODE REMAIN UP TO THE USER.

TABLE 6. SERIAL PORT CONTROL REGISTER / TIMER REGISTER

$$\text{Asynchronous Baud Rate} = \frac{2.5\ \text{MH:}}{64(PL + 1)(TL + 1)}$$

$$\text{Isosynchronous Baud Rate} = \frac{2.5\ \text{MH:}}{4(PL + 1)(TL + 1)}$$

where: PL = prescale latch value
TL = timer latch value

Example: To program the serial port to operate at 300 baud in the asynchronous mode, the prescaler value is set to 0, and the timer latch value to 81H.

MSB 7	6	5	4	3	2	1	LSB 0
X	1	0	0	0	0	PRE1	PRE0

PRE1, PRE0: 2 BIT PRESCALE LATCH VALUE (PL)

MSB 7	6	5	4	3	2	1	LSB 0
TIMER LATCH VALUE (TL)							

TABLE 7. ASCII CHARACTER SET ENCODED VALUES

LETTER	ENCODED VALUE (shown in Hexadecimal).	LETTER	ENCODED VALUE (shown in Hexadecimal).
A	21	N	2E
B	22	O	2F
C	23	P	30
D	24	Q	31
E	25	R	32
F	26	S	33
G	27	T	34
H	28	U	35
I	29	V	36
J	2A	W	37
K	2B	X	38
L	2C	Y	39
M	2D	Z	3A

TABLE 8. ALLOPHONE ADDRESS ENCODED VALUES (shown in Hexdecimal).

ENCODED VALUE	ALLPHONE	SAMPLE WORD	DURATION (as)	ENCODED VALUE	ALLPHONE	SAMPLE WORD	DURATION (as)
00	PA1	PAUSE	10	20	AW	OUt	250
01	PA2	PAUSE	30	21	DD2	Do	80
02	PA3	PAUSE	50	22	GG3	wiG	120
03	PA4	PAUSE	100	23	VV	Vest	130
04	PA5	PAUSE	200	24	GG1	Guest	80
05	OY	bOY	290	25	SH	SHip	120
06	AY	skY	170	26	ZH	aZUre	130
07	EH	End	50	27	RR2	bRain	80
08	KK3	Coab	80	28	FF	Food	110
09	PP	Pow	150	29	KK2	sKy	140
0A	JH	dodGe	400	2A	KK1	Can't	120
0B	NN1	thiN	170	2B	ZZ	Zoo	150
0C	IH	sIt	50	2C	NG	aNchor	200
0D	TT2	To	100	2D	LL	Lake	80
OE	RR1	Rural	130	2E	WW	Wool	140
0F	AX	sUceed	50	2F	XR	repaIR	250
10	MM	Milk	180	30	WH	WHig	150
11	TT1	parT	80	31	YY1	Yes	90
12	DH1	THey	140	32	CH	CHurch	150
13	IY	sEE	170	33	ER1	fIR	110
14	EY	bEIge	200	34	ER2	fIR	210
15	DD1	coulD	50	35	OW	bEAU	170
16	UW1	tO	60	36	DH2	THey	180
17	AO	OUght	70	37	SS	veST	60
18	AA	hOt	60	38	NN2	No	140
19	YY2	Yes	130	39	HH2	Hoe	130
1A	AE	hAt	80	3A	OR	stORe	240
1B	HH1	He	90	3B	AR	alARe	200
1C	BB1	Business	40	3C	YR	cleAR	250
1D	TH	THin	130	3D	GG2	Got	80
1E	UN	bOOk	70	3E	EL	saddLE	140
1F	UW2	fOOd	170	3F	BB2	Business	60

TABLE 9. PARALLEL PORT TIMING REQUIREMENTS:

SETUP TIME, BEFORE DATA CLOCK LO TO HI TRANSITION: MIN. 20 nS. HOLD TIME, BEFORE DATA CLOCK LO TO HI TRANSITION: MIN. 10 nS. WIDTH OF CLOCK LO: MIN. 500 nS.

HOLD OFF TIME, FROM DATA STROBE HI TO LOW TO HI, UNTIL NEXT DATA STROBE HI TO LOW: MIN. 450 uS.

NOTE: The addition of an 74LS74 Flip-Flop as shown on the schematic can be used for parallel port latch handshaking using the Active-LO LATCH-BUSY$ output. LATCH-BUSY$ is LO when the latch is full, and it is HI when the latch is empty and available for the next character to be strobed in.

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APPENDIX-A

Exception-Word Eprom Map (For use without USER eprom present)

NOTE: ENCAPSULATED SEQUENCES ARE USER-DEFINED, REFER TABLES 2,3, AND 4.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
X000	80	48	28	58	85	E0	35	E0	31	FF	FF	FF	FF	FF	FF	FF
X010	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
X020	FF	FF	FF	1E	1F	20	21	28	29	24	25	22	23	2A	2B	26
X030	27	2C	2D	2E	2F	32	33	34	35	36	E0	65	78	02	31	BE
X040	F1	43	C5	AA	X0	09	2D	FF	E2	1E	B8	AA	X0	23	D5	12
X050	D0	13	B9	9B	13	C3	AA	X0	09	2D	FF	E2	0B	B8	AA	X0
X060	23	D5	12	D0	13	B9	9B	13	5D	16	E6	E9	C3	AA	X0	09
X070	2D	FF	E2	14	A2	40	11	82	11	A2	15	11	C3	AA	X0	09
X080	82	15	C3	AA	X0	09	82	14	98	29	03	98	2B	07	22	20
X090	9B	03	BE	F7	2B	9B	03	05	98	07	09	98	03	19	8C	F1
X0A0	00	E0	36	X1	93	X1	AB	X1	A9	X1	B1	X1	B2	X1	B3	X1
X0B0	B4	X1	E1	X1	E2	X2	0D	X2	0E	X2	0F	X2	1B	X2	1C	X2
X0C0	1D	X2	1E	X2	2D	X2	2E	X2	2F	X2	30	X2	3D	X2	5A	X2
X0D0	5B	X2	64	X2	65	X2	6F	X2	70	D8	02	D8	03	98	03	11
X0E0	BE	F7	4B	8E	F7	0F	77	01	0A	05	74	80	0B	E0	03	73
X0F0	7F	0B	BE	F3	AF	76	20	0A	0E	52	34	AA	X0	A3	D0	14
X100	AA	X0	A4	D0	15	E0	0F	C5	2A	41	2C	02	AA	X0	A3	D0
X110	14	AA	X0	A4	D0	15	52	01	BE	F4	88	8E	F4	C2	76	10
X120	0A	4D	2D	FF	E2	60	98	11	1D	73	BF	0A	8E	F5	64	76
X130	10	0A	3C	8E	F4	7E	74	40	0A	8E	F5	64	76	10	0A	42
X140	48	37	34	79	00	35	D5	37	73	FD	0B	52	02	8E	F4	88
X150	8E	F4	9E	98	0F	03	98	03	11	8E	F7	4B	77	80	0B	0A
X160	DB	39	8E	F3	47	C9	C9	8C	F1	36	C9	C9	8C	F3	F4	D3
X170	15	E7	02	D3	14	52	02	8E	F4	88	72	01	37	73	FD	0B
X180	E0	99	52	03	E0	F1	D9	03	D9	02	D5	37	73	FD	0B	8C
X190	F3	EE	FF	13	6E	24	B9	13	5A	0B	01	21	13	00	12	0F
	P	P		>[A N D Y] > [AENNIP PP2 IY P DH AX												
X1A0	00	01	41	22	27	14	8D	FF	FF	13	61	B0	21	6A	14	89
X1B0	FF	FF	FF	FF	13	E9	13	4A	07	0B	33	3E	00	0C	0B	37
X1C0	0D	27	1F	10	07	0B	02	BD	13	E9	2D	21	29	2C	13	4A
X1D0	07	0B	33	3E	00	0C	0B	37	0D	27	1F	10	07	0B	02	8D
X1E0	FF	FF	13	E4	13	46	00	21	07	0B	02	0D	0C	28	0C	02
X1F0	2A	14	25	0F	BB	13	73	2C	A5	13	46	01	BE	13	73	2C
X200	21	2E	A4	13	46	00	2D	1A	0B	01	15	01	FF	FF	FF	13
X210	69	36	25	A4	13	6D	0C	23	03	95	FF	FF	FF	FF	13	75
X220	32	30	2F	33	A5	13	49	33	09	0F	37	B7	FF	FF	FF	FF
X230	13	6F	34	21	AC	13	4D	35	0D	00	0F	BE	FF	13	73	25
X240	32	29	A4	13	71	16	2B	33	01	06	00	21	07	0B	02	0D
X250	0C	28	0C	02	2A	14	25	0F	BB	FF	FF	13	65	07	32	A5
X260	6E	13	B4	FF	FF	13	6F	35	07	32	A5	13	59	BA	FF	FF
X270	13	CF	13	59	3A	01	10	07	37	37	0C	01	0A	00	02	2A
X280	1A	0B	01	3F	13	00	37	37	02	09	35	02	2A	07	0B	00
X290	2E	0C	1D	00	12	0F	00	02	0D	0F	02	32	00	0F	23	00
X2A0	14	00	02	2A	13	80	C6	5A	0B	15	80	FF				
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

←sample NEW PARAMETERS. (see table 2).

←NEW PARAMETER INITIALIZATION ROUTINE.

The MSnibble of the following locations from the NEW PARAMETER INITIALIZATION ROUTINE are user defined also: X044,X04C,X057,X05F,X06E,X07E,and X084; where X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E.

←sample ALPHABETIZED EXCEPTION-WORD INDEX, where X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E. (see table 3).

←EXCEPTION-WORD ROUTINE.

The MSnibble of the following locations from the EXCEPTION-WORD ROUTINE are user defined also: X0FC,X101,X10D,and X112; where X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E.

←sample ENCODED EXCEPTION-WORDS. (see table 4).

(see APPENDIX-C for discussion of encoding scheme.)

—YOUR EXCEPTION-WORD EPROM CAN RESIDE ANYWHERE FROM 1000H TO E000H, PROVIDING IT BEGINS ON A 4K BOUNDARY WHERE X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E.

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APPENDIX-B

Exception-Word Eprom Map (For use without USER eprom present)

NOTE: ENCAPSULATED SEQUENCES ARE USER-DEFINED, REFER TABLES 2,3, AND 4.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
X000	80	48	28	58	85	E0	35	E0	31	FF	FF	FF	FF	FF	FF	FF	←sample NEW PARAMETERS. (see table 2).
X010	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	
X020	FF	FF	FF	1E	1F	20	21	28	29	24	25	22	23	2A	2B	26	←NEW PARAMETER INITIALIZATION ROUTINE. The MSnibble of the following locataions from the NEW PARAMETER INITIALIZATION ROUTINE are user defined also: X044,X04C,X057,X05F,X06E,X07E,and X084; where X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E.
X030	27	2C	2D	2E	2F	32	33	34	35	36	E0	65	78	02	31	BE	
X040	F1	43	C5	AA	X0	09	2D	FF	E2	1E	B8	AA	X0	23	D5	12	
X050	D0	13	B9	9B	13	C3	AA	X0	09	2D	FF	E2	0B	B8	AA	X0	
X060	23	D5	12	D0	13	B9	9B	13	5D	16	E6	E9	C3	AA	X0	09	
X070	2D	FF	E2	14	A2	40	11	82	11	A2	15	11	C3	AA	X0	09	
X080	82	15	C3	AA	X0	09	82	14	98	29	03	98	2B	07	22	20	
X090	9B	03	BE	F7	2B	9B	03	05	98	07	09	98	03	19	8C	MS	←(see note 1 below).
X0A0	LS	E0	36	X1	93	X1	AB	X1	A9	X1	B1	X1	B2	X1	B3	X1	←sample ALPHABETIZED EXCEPTION-WORD INDEX, where X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E. (see table 3).
X0B0	B4	X1	E1	X1	E2	X2	0D	X2	0E	X2	0F	X2	1B	X2	1C	X2	
X0C0	1D	X2	1E	X2	2D	X2	2E	X2	2F	X2	30	X2	3D	X2	5A	X2	
X0D0	5B	82	64	82	65	82	6F	82	70	D8	02	D8	03	98	03	11	←EXCEPTION-WORD ROUTINE.
X0E0	BE	F7	4B	8E	F7	0F	77	01	0A	05	74	80	0B	E0	03	73	
X0F0	7F	0B	BE	F3	AF	76	20	0A	0E	52	34	AA	80	A3	D0	14	The MSnibble of the following locations from the EXCEPTION-WORD ROUTINE are user defined also: X0FC,X101,X10D,and X112; where X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E.
X100	AA	80	A4	D0	15	E0	0F	C5	2A	41	2C	02	AA	80	A3	D0	
X110	14	AA	80	A4	D0	15	52	01	BE	F4	88	8E	F4	C2	76	10	
X120	0A	4D	2D	FF	E2	60	98	11	1D	73	BF	0A	BE	F5	64	76	
X130	10	0A	3C	8E	F4	7E	74	40	0A	8E	F5	64	76	10	0A	42	
X140	48	37	34	79	00	33	D5	37	73	FD	0B	52	02	8E	F4	88	
X150	8E	F4	9E	98	0F	03	98	03	11	8E	F7	4B	77	80	0B	0A	
X160	DB	39	BE	F3	47	C9	C9	8C	F1	36	C9	C9	8C	F3	F4	D3	
X170	15	E7	02	D3	14	52	02	BE	F4	88	72	01	37	73	FD	0B	
X180	E0	99	52	03	E0	F1	D9	03	D9	02	D5	37	73	FD	0B	8C	
X190	F3	EE	FF	13	6E	24	B9	15	5A	0B	01	21	13	00	12	0F	←sample ENCODED EXCEPTION-WORDS. (see table 4).
X1A0	00	01	41	22	27	14	8D	FF	FF	13	61	B0	21	6A	14	89	
X1B0	FF	FF	FF	FF	13	E9	13	4A	07	0B	33	3E	00	0C	0B	37	
X1C0	0D	27	1F	10	07	0B	02	8D	13	E9	2D	21	29	2C	13	4A	
X1D0	07	0B	33	3E	00	0C	0B	37	0D	27	1F	10	07	0B	02	BD	
X1E0	FF	FF	13	E4	13	46	00	21	07	0B	02	0D	0C	2B	0C	02	
X1F0	2A	14	25	0F	BB	13	73	2C	A5	13	46	01	BE	13	73	2C	
X200	21	2E	A4	13	46	00	2D	1A	0B	01	15	01	FF	FF	FF	13	(see APPENDIX-C for discussion of encoding scheme).
X210	69	36	25	A4	13	6D	0C	23	03	95	FF	FF	FF	FF	13	75	
X220	32	30	2F	33	A5	13	49	33	09	0F	37	B7	FF	FF	FF	FF	
X230	13	6F	34	21	AC	13	4D	35	0D	00	0F	BE	FF	13	73	25	
X240	32	29	A4	13	71	16	2B	33	01	06	00	21	07	0B	02	0D	
X250	0C	28	0C	02	2A	14	25	0F	BB	FF	FF	13	65	07	32	A5	
X260	6E	13	B4	FF	FF	13	6F	35	07	32	A5	13	59	BA	FF	FF	
X270	13	CF	13	59	3A	01	10	07	37	37	0C	01	0A	00	02	2A	
X280	1A	0B	01	3F	13	00	37	37	02	09	35	02	2A	07	0B	00	
X290	2E	0C	1D	00	12	0F	00	02	0D	0F	02	32	00	0F	23	00	
X2A0	14	00	02	2A	13	80	C6	5A	0B	15	80	FF					

NOTE: 1. APPENDIX-B is the same as APPENDIX-A, except for two address. These are X09F and X0A0 (MSB and LSB respectively, labeled MS and LS above). Place the origin of the MAIN-CONTROL-PROGRAM (see APPENDIX-F) in these locations so that program control will transfer to the user's code at the appropriate time.

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APPENDIX-C

Exception-Word Encoding Scheme

To store a unique word or symbol and its corresponding allophone address string in an efficient and flexible manner, the following encoding format was derived:

<[encoded word or symbol]< = [encoded allophone address(es)]

where: < equals 13H.
[equals 40H.
] equals 80H.

The first and lasty byte is 13H. This informs the code-to-speech algorithm that the word or symbol is not a prefix or suffix.

If the word or symbol is an individual letter, then the representation of it between the brackets is an FFH; this includes the value of the left and right brackets.

Otherwise:
(1) The first letter in the word or symbol is always to be ignored.
(2) The next letter in the word is represented by the value of the letter from TABLE-7, plus the value of the left bracket "[" which is 40H.
(3) The following letter(s), if and only if it is not the last letter in the word or symbol, is represented solely by its value from TABLE-7.
(4) The last letter in the word or symbol is represented by the value of the letter from TABLE-7, plus the value of the right bracket "]" which is 80H.

The allophone address string is encoded in a similar manner:

If only one allophone is used for the pronunciation, it is represented by its value from TABLE-6, plus the value of the right "[" and left "]" brackets which are 40H and 80H respectively.

Otherwise:
(1) The first allophone is represented by its value from TABLE-8, plus the value of the left bracket "[" which is 40H.
(2) The following allophone(s), if and only if it is not the last allophone in the string, is represented by its value from TABLE-8.
(3) The last allophone is represented by its value from TABLE-8 plus the value of the right bracket "]" which is 80H.

Example: To encode "Au" to pronounce as "GOLD"
<[Au]< = [GG2 0W LL DD1]
13,F5,13, 7D, 35,2D,95 ←This line is ready to store in EXCEPTION-WORD epros under the "A" category.
↑ (The encoded string is shown in Hexadecimal notation.)
—Remember, throw away the first letter (in this case an "A"), then find the value of the next letter in TABLE-7 and add 40H plus 80H to it so as to represent the left "[" and right "]" brackets.

APPENDIX-D

User Eprom Map (For use without EXCEPTION-WORD eprom)

NOTE: ENCAPSULATED SEQUENCES ARE USER-DEFINED, REFER TABLES 2,3, AND 4.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
X000	80	48	28	58	85	E0	35	E0	31	FF	FF	FF	FF	FF	FF	FF	←sample NEW PARAMETERS.
X010	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	(see table 1).
X020	FF	FF	FF	1E	1F	20	21	28	29	24	25	22	23	2A	2B	26	←NEW PARAMETER INITIALIZATION
X030	27	2C	2D	2E	2F	32	33	34	35	36	E0	65	78	02	31	BE	ROUTINE.
X040	F1	43	C5	AA	X0	09	2D	FF	E2	1E	B8	AA	X0	23	D5	12	The MSnibble of the following locations
X050	D0	13	B9	9B	13	C3	AA	X0	09	2D	FF	E2	0B	B8	AA	X0	from the NEW PARAMETER INITIALIZATION
X060	23	D5	12	D0	13	B9	9B	13	5D	16	E6	E9	C3	AA	X0	09	ROUTINE are user defined also:
X070	2D	FF	E2	14	A2	40	11	82	11	A2	15	11	C3	AA	X0	09	X044,X04C,X057,X05F,X06E,X07E,and X084;
X080	82	15	C3	AA	X0	09	82	14	98	29	03	98	2B	07	22	20	where X = 1,2,3,4,5,6,7,8,9,A,B,C,D,or E.
X090	9B	03	BE	F7	2B	9B	03	05	98	07	09	98	03	19	8C	MS	←(see note A on following page).

APPENDIX-D (Cont'd)

```
X0A0 LS 8C F3 F4
        User code may start at X0A4,
        but must contain the MAIN-CONTROL-PROGRAM
        somewhere within, refer to APPENDIX-F.
```

NOTE A. Place the immediate address of the origin of the MAIN-CONTROL-PROGRAM (see APPENDIX-F) in these locations; so that program control will transfer to the user's code at the appropriate time.

APPENDIX-E

USER EPROM MAP (For use with EXCEPTION-WORD eprom)

NOTE 1. Contains no reserved locations, except for the MAIN-CONTROL-PROGRAM. (See APPENDIX-F).

NOTE 2. A user's code does not have to reside in a second eprom (USER eprom). It may reside in an unused portion of an EXCEPTION-WORD eprom which is for use where "USER eprom is present". Refer APPENDIX-B.

APPENDIX-F

USER's MAIN CONTROL PROGRAM (For residency anywhere within USER eprom).

NOTE: ENCAPSULATED AREAS ARE USER DEFINED UNLESS OTHERWISE NOTED.

```
F1AC =     AUDIBLE    EQU 0F1ACH   ;< ——
F3E7 =     GISPEECH   EQU 0F3E7H   ;< ——  THESE ARE ADDRESS VECTORS WITHIN
F1E2 =     SAVE       EQU 0F1E2H   ;< ——  THE MASKED CODE-TO-SPEECH ALGORITHM.
F1F0 =     ESCAPE     EQU 0F1F0H   ;< ——
000B =     F2         EQU R11
0002 =     F1HI       EQU R2
0003 =     F1LO       EQU R3
0004 =     R1HI       EQU R4
0005 =     R1LO       EQU R5
0007 =     F2LO       EQU R7
0009 =     R2LO       EQU R9
0038 =     WORDCNTH   EQU R56
0039 =     WORDCNTL   EQU R57
0032 =     BUFBVALU   EQU R50
0000 =     IOCNT0     EQU P0

9000       ORG > 9000        ;This is the origin of the Main Control Program which is defined by the user.
                             ;Here it is arbitrarily chosen to be 9000H. Remember to place this immediate
                             ;address in the "MS","LS" locations of the EXCEPTION-WORD eprom ("for use
                             ;with USER eprom"), see APPENDIX-B. (MS = MSB = 90 and the LS = LSB = 00 in
                             ;this example.)
9000 BEF1AC   MESSAGE: CALL @AUDIBLE
+ ———————— THIS ENCAPSULATED AREA IS NOT USER DEFINED ———————— +
| The following two lines are placed here only if the user code wishes to gain   |
| access to the serial port.                                                      |   (The XXXX XXXX here does
                                                                                       not have the same meaning
| XXXX XXXX          ANDP %>FE,IOCNT1    ;DISABLE INTERRUPT-4 (SERIAL                  as the X from the previous
                                          PORT).                                  |    appendices and tables.)

| XXXX XXXX          ANDP %FE,PORTB      ;SET BUSY* LO.                           |
+ ———————————————————————————————————————————————————————————————————————————————— +
9003 E00E                JMP ANYSTART

9005 BC9046   CRSTART:   BR @USERCODE    ;THE BRANCH ADDRESS BELOW IS USER DEFINED.
                                         ;AFTER INITIALIZATION OR AFTER PROCESSING AND
                                         ;SPEAKING WHAT HAS BEEN LOADED INTO THE INPUT
                                         ;BUFFER CONTROL TRANSFERS TO THE USER CODE VIA THIS
                                         ;BRANCH INSTRUCTION.
```

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APPENDIX-F (Cont'd)

```
900B 76010B07   SPEAK:      BTJO %>01,F2,ANYSTART
900C 73EF0B                 AND %>EF,F2
900F 77100BFC   CRWAIT:     BTJZ %10,F2,CRWAIT
9013 4D0305     ANYSTART:   CMP F1LO,R1LO
9016 E607                   JNE HOLEWORD
9018 4D0204                 CMP F1HI,R1HI
901B E602                   JNE HOLEWORD
901D E0E6                   JMP CRSTART
901F 7D0038     HOLEWORD:CMP %>00,WORDCNTH
9022 E605                   JNE BFULTEST
9024 7D0039                 CMP %>00,WORDCNTL
9027 E2F6                   JEQ HOLEWORD
9029 770B0B09   BFULTEST:   BTJZ %>08,F2,PROCESS
902D 7D0132     LOCKUP:     CMP %>01,BUFBVALU
9030 E211                   JEQ ESC
9032 760B0BFC   BFULHOLD:   BTJO %>08,F2,BFULHOLD
9036 BEF3D7     PROCESS:    CALL @GISPEECH
9039 4DO709     MAINROUT:   CMP F2LO,R2LO
903C E205                   JEQ ANYSTART
903E A40100                 DRP %>01,1OCNT0
9041 E0D0                   JMP ANYSTART
9043 BCF1F0     ESC:        BR @ESCAPE

9046 00         USERCODE: NOP   ;FROM THIS POINT IT IS THE USER CODES RESPONSIBILITY
                                ;TO EXECUTE ITS OWN CODE OR TO LOAD A CHARACTER
                                ;STRING INTO THE INPUT BUFFER.
                                ;THE TWO EXAMPLES SHOWN BELOW DEMONSTRATE THE
                                ;RECOMMENDED SEQUENCE OF EVENTS FOR EACH MODE.
                                ;MODE 1 IS USED WHEN THE USER CODE HAS PREVIOUSLY
                                ;PREPARED THE CHARACTER STRING IT WISHES TO HAVE
                                ;SPOKEN; MODE 2 IS USED WHEN THE USER CODE WISHES
                                ;TO EXECUTE ANYTHING ELSE.
                                ;
                MODE1:          ;LOADING INPUT BUFFER OF CODE-TO-SPEECH ALGORITHM:
                                ;
                                ;ACCUMULATOR AND STATUS REGISTER ARE TO BE SAVED.
                                ;NO OTHER REGISTER IS TO BE MODIFIED.
                                ;Loading a character string is accomplished
                                ;by placing each character into the Accumulator and
                                ;then using CALL @SAVE to load it into the input
                                ;buffer. Remember to end each word or phrase with a
                                ;delimeter. Restore the Accumulator and the Status Registers. Call @SPEAK to
                                ;process
                                ;and speak the word(s) or phrase(s) that were loaded.
                                ;
```

NOTE: Once "SPEAK" is initiated, control does not return to the USERCODE until the last word or phrase that is in the input buffer has been processed by the code-to-speech algorithm. NOTE: Because of masked code-to-speech restrictions, the USER can not intercept input from the serial port while speech processing is in progress. During this interval, handshaking (BUSY*) shall hold off additional serial communication. This is accomplished by the two encapsulated lines shown above.

```
                                ;
                                ;THE FOLLOWING EXAMPLE WILL LOAD THE LETTER "A" AND
                                ;SPEAK IT:

9047  0E        PUSH ST         ;SAVE CONTENTS OF STATUS REGISTER.
9048  B8        PUSH A          ;SAVE CONTENTS OF ACCUMULATOR.
9049  2241      MOV %>41,A      ;MOVE 41H (which is ASCII "A") into the ACCUMULATOR.
904B  8EF1E2    CALL @SAVE      ;LOAD THE ASCII "A" INTO THE INPUT BUFFER.
904E  222D      MOV %>0D,A      ;MOVE 0DH (which is a carriage return).
9050  BEF1E2    CALL @SAVE      ;LOAD THE DELIMETER INTO THE INPUT BUFFER.
9053  B9        POP A           ;RECOVER CONTENTS OF ACCUMULATOR.
9054  08        POP ST          ;RECOVER CONTENTS OF STATUS REGISTER.
9055  8C900B    BR @SPEAK       ;TRANSFER CONTROL TO THE MAIN-CONTROL-PROGRAM WHICH

                                ;WILL ACCESS THE CODE-TO-SPEECH ALGORITHM; AFTER WHICH
                                ;THE CONTROL WILL RETURN TO THE "BR @USERCODE" INSTRUCTION
                                LOCATION.
```

APPENDIX-F (Cont'd)

```
9058 00    MODE2: NOP          ;
                               ;The following is the recommended
                               ;sequence of events necessary for the user's code
                               ;to do anything else (except for loading the input
                               ;buffer as described under MODE 1.)
                               ;
                               ;SAVE STATUS REGISTER
                               ;SAVE REGISTER 0 THRU 39H (EXTERNAL-RAM MODE), along with 3AH thru
                               ;current Stack Pointer.
                               ;OR, SAVE REGISTER 0 THRU 7FH (INTERNAL-RAM MODE).
                               ;(DO NOT USE PUSH INSTRUCTIONS TO SAVE THE REGISTERS BECAUSE
                               ;THE STACK IS NOT LARGE ENOUGH, INSTEAD
                               ;BLOCK MOVE THE RESPECTIVE REGISTER CONTENTS INTO
                               ;EXTERNAL-USER-RAM.
                               ;
                               ;USER DEFINED CODE GOES HERE NEXT.
                               ;
                               ;(TO READ THE SERIAL PORT, SEE THE EXAMPLE SEQUENCE BELOW).
                               ;
                               ;THEN RECOVER RESPECTIVE REGISTERS.
                               ;RECOVER STATUS REGISTER.
                               ;BRANCH TO MODE 1, OR BRANCH TO OTHER USER CODE such as the
                               ;example shown below
                               ;for reading the serial port.
                               ;The following is the recommended sequence of events necessary
                               ;for the user's code to obtain input from the serial port:
                               ;
LOOP:   DRP %>01,IOCNT1        ;ENABLE INTERRUPT-4 (SERIAL PORT) BECAUSE WANT TO RECEIVE SERIAL
                               ; INPUT.
        DRP %>01,PORTB         ;SET BUSY$ HI.
        IDLE                   ;WAIT HERE FOR SERIAL INTERRUPT TO OCCUR AND TO BE SERVICED.
        ANDP %>FE,IOCNT1       ;DISABLE INTERRUPT-4 (SERIAL PORT).

                               ;
     NOP                       ;THE CHARACTER RECEIVED BY SERIAL PORT IS IN THE ACCUMULATOR,
                               ;SO THE USER MAY EVALUATE IT HERE.
                               ;
     MOV %>08,A                ;LOAD A "BACKSPACE" INTO ACCUMULATOR IN ORDER TO TELL
     CALL @SAVE                ;THE CODE-TO-SPEECH INPUT BUFFER TO IGNORE THE CHARACTER
                               ;WHICH ARRIVED VIA THE SERIAL PORT.
                               ;

     NOP                       ;IF USER WANTS ADDITIONAL CHARACTERS FROM THE SERIAL PORT TO

                               ;EVALUATE:
                               ;JUMP TO LOOP TO WAIT FOR NEXT SERIAL PORT INTERRUPT (JMP LOOP).
                               ;
                               ;OTHERWISE: ENABLE INTERRUPT-4 (DRP %>01,IOCNT1), SET BUSY$ LO
                               ;(ANDP %>FE,PORTB),
                               ;THEN FALL THRU TO REST OF USER CODE.
```

NOTE: To successfully incorporate a USER program with the code-to-speech algorithm requires a thorough understanding of the concepts described in this application note, and an in-depth working knowledge of PIC7001 assembly language.

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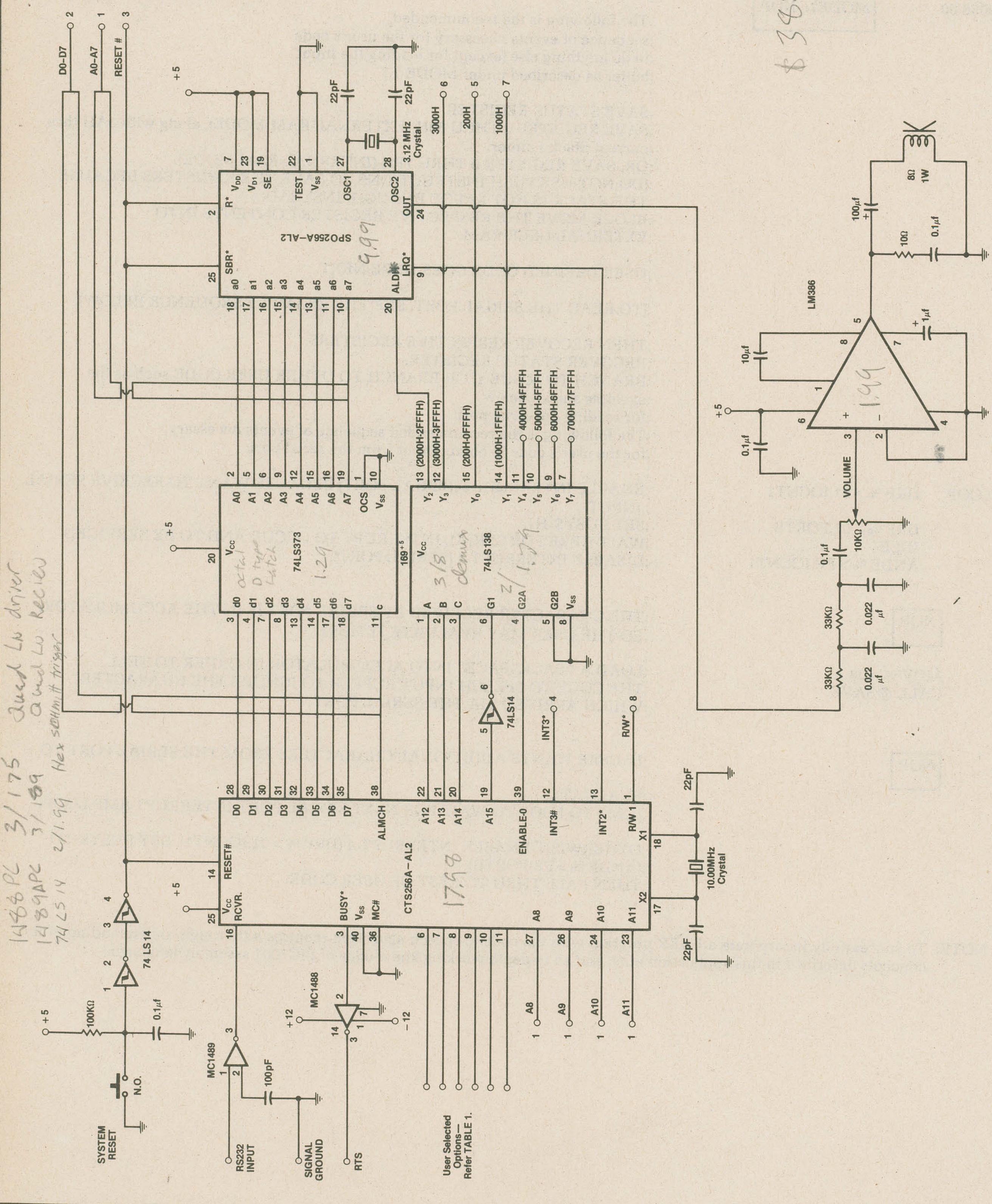
TYPICAL APPLICATION



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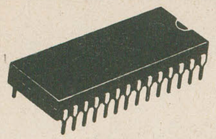


SPEECH PROCESSOR SP0256
276-1784

GENERAL DESCRIPTION

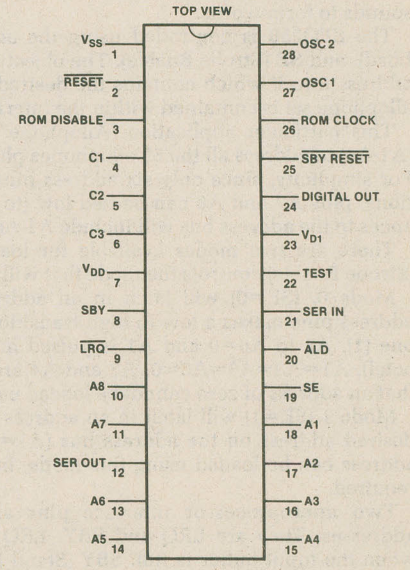
The SPO256 (Speech Processor) is a single chip N-Channel MOS LSI device that is able, using its stored program to synthesize speech or complex sounds.

The achievable output is equivalent to a flat frequency response ranging from 0 to 5KHz, a dynamic range of 42dB, and a signal to noise ratio of approximately 35 dB.

The SPO256 incorporates four basic functions:

A. A software programable digital filter that can be made to model a VOCAL TRACT.
B. A 16K ROM which stores both data and instructions (THE PROGRAM).
C. A MICROCONTROLLER which controls the data flow from the ROM to the digital filter, the assembly of the "word settings" necessary for linking speech elements together, and the amplitude and pitch information to excite the digital filter.
D. A PULSE WIDTH MODULATOR that creates a digital output which is converted to an analog signal when filtered by an external low pass filter.

PIN CONNECTION



FEATURES

- Natural Speech
- Wide Operating Voltage
- Simple Interface to Most Microcomputers or Microprocessors
- Supports L.P.C. Synthesis: Formant Synthesis: Allophone Synthesis

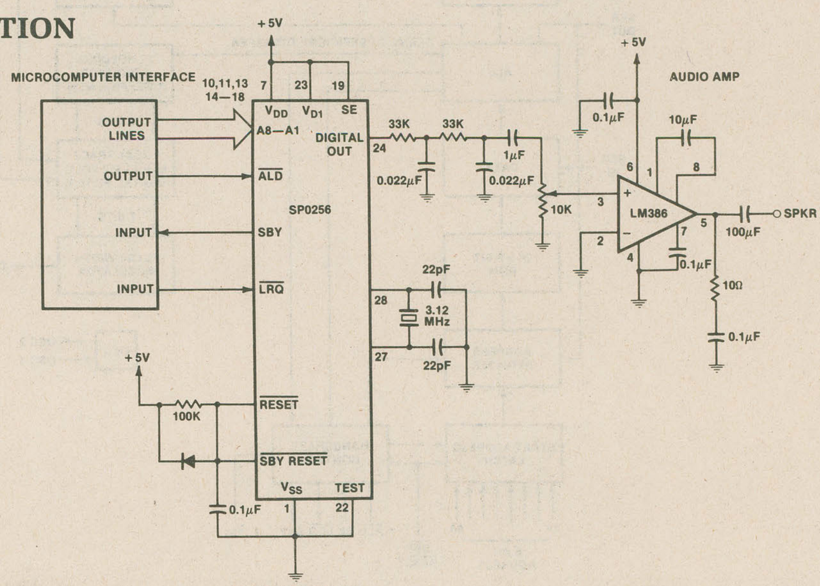
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD})	7 V
(V_{D1})	7 V
All Pins With Respect to V_{SS})	−0.3 To 8 V
Supply Current (I_{DD}) (V_{D1}, V_{DD}=7V) (Reset and SBY Reset High)	90 mA
Supply Current (I_{D1} (V_{D1}, V_{DD}=7V) (Reset and SBY Reset High)	21 mA
Storage Temperature Range	−25°C To 125°C
Operating Temperature Range	0°C To 70°C

STANDARD CONDITIONS

Clock-Crystal Frequency	3.120 MHz

TYPICAL APPLICATION



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ALLOPHONE USAGE WITH A MICROPROCESSOR

The SPO256 requires the use of a processor to concatenate the speech sounds to form words.

The SPO256 is controlled using the address pins (A1-A8), ALD (Address Load), and SE (Strobe Enable). The object for controlling the chip is to load an address into it which contains the desired allophone. The speech data for the allophone set is contained within the internal 16 K ROM of the SPO256.

This particular application (Allophone Set) requires only six address pins (A1-A6) to address all the 59 allophones plus five pauses, a total of 64 locations. For simplicity, since only six address pins are needed to address the 64 locations, pins A7 and A8 can be tied low (to ground) and now any further references to the address bus will include A1-A6 and A7=A8=0.

There are two modes available for loading an address into the chip. SE (Strobe Enable) controls the mode that will be used.

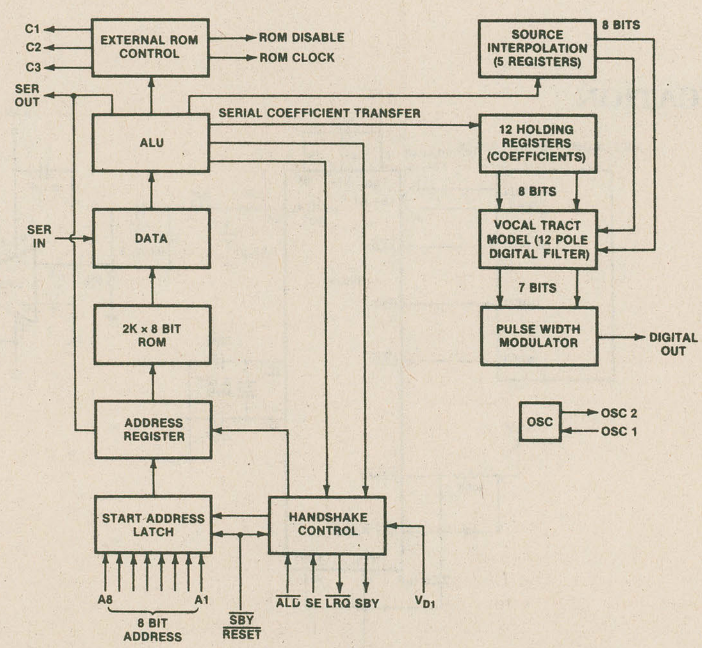
Mode 0. (SE=0) will latch in an address when any one or more of the address pins makes a low to high transition. For example, to load the address one (1), A2 to A6=0 and A1 is pulsed high. To load the address twelve (12 octal), A1=A3=A5=A6=0, A2 and A4 are pulsed high simultaneously. (Note that an address of zero cannot be loaded using this mode).

Mode 1 (SE=1) will latch in an address using the ALD pin. First, setup the desired address on the address bus (A1=A6) and then pulse ALD low. Any address can be loaded using this mode, but certain setup and hold times are required.

Two microprocessor interface pins are available for quick loading of addresses. They are LRQ and SBY. LRQ (Load Request) tells the processor when the input buffer is full. SBY (Stand By) tells the processor that the chip has stopped talking and no new address has been loaded. Either interface pin can be used when concatenating allophones. LRQ is an active low signal, when LRQ goes low it is time to load a new address to the chip. If LRQ is high, then simply wait for it to go low before loading the address. SBY will stay high until an address is loaded, then it will go low and stay low until all the internal instructions (Speech Code) from that one address are completed. Once this signal goes high, it is time to load a new address. Since speech does not require very fast address loading, it would be acceptable to use SBY to interface to the processor.

To end a word using allophones it is necessary to load a pause to complete the word. For example, the word "TWO" can be implemented using the following allophones, TT2-VW2-PA1. PA1 is actually not an allophone but a pause which is needed to end the word.

BLOCK DIAGRAM



ALLOPHONE BASED SPEECH PROCESSOR—SP0256-AL2

PIN FUNCTIONS

PIN NUMBER	NAME	FUNCTION
1	V_{SS}	Ground
2	$\overline{\text{RESET}}$	A logic 0 resets that portion of the SP powered by V_{DD}. Must be returned to a logic 1 for normal operation.
3	ROM DISABLE	For use with an external serial speech ROM, a logic 1 disables the external ROM.
4, 5, 6	C1, C2, C3	Output control lines for use with an external serial speech ROM.
7	V_{DD}	Power supply for all portions of the SP except the microprocessor interface logic.
8	SBY	STANDBY. A logic 1 output indicates that the SP is inactive and V_{DD} can be powered down externally to conserve power. When the SP is reactivated by an address being loaded, SBY will go to a logic 0.
9	$\overline{\text{LRQ}}$	$\overline{\text{LOAD REQUEST}}$. $\overline{\text{LRQ}}$ is a logic 1 output whenever the input buffer is full. When $\overline{\text{LRQ}}$ goes to a logic 0, the input port may be loaded by placing the 8 address bits on A1-A8 and pulsing the $\overline{\text{ALD}}$ output.
10, 11, 13, 14, 15, 16, 17, 18,	A8, A7, A6, A5, A4, A3, A2, A1	8 bit address which defines any one of 256 speech entry points.
12	SER OUT	SERIAL ADDRESS OUT. This output transfers a 16-bit address serially to an external speech ROM.
19	SE	STROBE ENABLE. Normally held in a logic 1 state. When tied to ground, $\overline{\text{ALD}}$ is disabled and the SP will automatically latch in the address on the input bus approximately 1μs after detecting a logic 1 on any address line.
20	$\overline{\text{ALD}}$	$\overline{\text{ADDRESS LOAD}}$. A negative pulse on this input loads the 8 address bits into the input port. The negative edge of this pulse causes $\overline{\text{LRQ}}$ to go high.
21	SER IN	SERIAL IN. This is an 8-bit serial data input from an external speech ROM.
22	TEST	This pin should be grounded for normal operation.
23	VD1	Power supply for the microprocessor interface logic and controller.
24	DIGITAL OUT	Pulse width modulated digital speech output which, when filtered by a 5KHz low pass filter and amplified, will drive a loudspeaker.
25	$\overline{\text{SBY RESET}}$	$\overline{\text{STANDBY RESET}}$. A logic 0 resets the microprocessor interface logic and the address latches. Must be returned to a logic 1 for normal operation.
26	ROM CLOCK	This is a 1.56MHz clock output used to drive an external serial speech ROM.
27	OSC1	XTAL IN. Input connection for a 3.12MHz crystal.
28	OSC2	XTAL OUT. Output connection for a 3.12MHz crystal

ALLOPHONE SPEECH SYNTHESIS

INTRODUCTION

The allophone speech synthesis technique provides the user with the ability to synthesize an unlimited vocabulary at a very low bit rate. Fifty-nine discrete speech sounds (called allophones) and five pauses are stored at different addresses in the SPO256 internal ROM. Each speech sound was excised from a word and analyzed using linear predictive coding (LPC). Any English word or phrase can be created by addressing the appropriate combination of allophones and pauses. Since there is a total of 64 address locations each requires a 6 bit address. Assuming that speech contains 10 to 12 sounds per second, allophone synthesis requires addressing less than 100 bits per second.

LINGUISTICS

A few basic linguistic concepts will help you start your own library of "allophone words". (See Table 1 for Allophone Dictionary). First, there is no one-to-one correspondence between written letters and speech sounds; secondly, speech sounds are acoustically different depending upon their position within

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LINGUISTICS (Continued)

a word; and lastly, the human ear may perceive the same acoustic signal differently in the context of different sounds.

The first point compares to the problem that a child encounters when learning to read. Each sound in a language may be represented by more than one letter and, conversely each letter may represent more than one sound. (See the examples in Table 2.) Because of these spelling irregularities, it is necessary to think in terms of *sounds*, not letters, when using allophones.

The second, and equally important, point to understand, is that the acoustic signal of a speech sound may differ depending upon its position within a word. For example, the initial *K* sound in *coop* will be acoustically different from the *K*'s in *keep* and *speak*. The *K*'s in *coop* and *keep* differ due to the influence of the vowels which follow them, and the final *K* in speak is usually not as loud as initial *K*'s.

Finally, a listener may identify the same acoustic signal differently depending on the context in which it is perceived. Don't be surprised, therefore, if an allophone word sounds slightly different when used in various phrases.

PHONEMES OF ENGLISH

The sounds of a language are called phonemes, and each language has a set which is slightly different from that of other languages. Table 3 contains a chart of all the consonant phonemes of English, table 4 all the vowel phonemes.

Consonants are produced by creating an occlusion or constriction in the vocal tract which produces an aperiodic sound source. If the vocal cords are vibrating at the same time, as in the case of the voiced fricatives VV, DH, ZZ, and ZH, (See Table 5) there are two sound sources: one which is aperiodic and one which is periodic.

Vowels are usually produced with a relatively open vocal tract and a periodic sound source provided by the vibrating vocal cords. They are classified according to whether the front or back of the tongue is high or low (See Table 4) whether they are long or short, and whether the lips are rounded or unrounded. In English all rounded vowels are produced in or near the back of the mouth (UW, UH, OW, AO, OR, AW).

Speech sounds which have features in common behave in similar ways. For example, the voiceless stop consonants PP, TT and KK (See Table 3) should be preceded by 50-80 msec of silence, and the voiced stop consonants BB, DD, and GG by 10-30 msec of silence.

ALLOPHONES

Phoneme is the name given to a group of similar sounds in a language. Recall that a phoneme is acoustically different depending upon its position within a word. Each of these positional variants is an allophone of the same phoneme. An allophone, therefore, is the manifestation of a phoneme in the speech signal. It is for this reason that our inventory of English speech sounds is called an allophone set.

HOW TO USE THE ALLOPHONE SET

(See Table 1 for instructions on how to create all the sample words mentioned in this section.) The allophone set (Refer to Table 5) contains two or three versions of some phonemes. It may be necessary to use one allophone of a particular phoneme for word-or-syllable-final position. A detailed set of guidelines for using the allophones is given in Table 5. Note that these are suggestions, not rules.

For example, DD2 sounds good in initial position and DD1 sounds good in final position, as a "daughter" and "collide." One of the differences between the initial and final versions of a consonant is that an initial version may be longer than the final version. Therefore, to create an initial SS, you can use two SSs instead of the usual single SS at the end of a word or syllable, as in "sister." Note that this can be done with TH and FF, and the inherently short vowels (to be discussed below), but with no other consonants. You will want to experiment with some consonant clusters (strings of consonants such as *str, cl*) to discover which version works best in the cluster. For example, KK1 sounds good before LL as in "clown," and KK2 sounds good before WW as in "square." One allophone of a particular phoneme may sound better before or

HOW TO USE THE ALLOPHONE SET (Continued)

after back vowels and another before or after front vowels. KK3 sounds good before UH and KK1 sounds good before IY, as in "cookie." Some sounds (PP, BB, TT, DD, KK, GG, CH, and JH) require a brief duration of silence before them. For most of these, the silence has already been added but you may decide you want to add more. Therefore, there are several pauses included in the allophone set varying from 10–200 msec. To create the final sounds in the words "letter" and "little" use the allophone ER and EL.

Remember that you must always think about how a word *sounds*, not how it is spelled. For example, the NG sound is represented by the letter N in "uncle". And remember that some sounds may not even be represented in words by any letters, as the YY in "computer".

As mentioned earlier there are some vowels which can be doubled to make longer versions for stressed syllables. These are the inherently short vowels IH, EH, EA, EX, AA, and UH. For example, in the word "extent" use one EH in the first syllable, which is unstressed and two EHs in the second syllable which is stressed. Of the inherently long vowels there is one, UW, which has a long and short version. The short one, UW1, sounds good after YY in computer. The long version, UW2, sounds good in monosyllabic words like "two." Included in the vowel set is a group called R-colored vowels. These are vowel + R combinations. For example, the AR in "alarm" and the OR in "score." Of the R-colored vowels there is one, ER, which has a long and short version. The short version is good for polysyllabic words with final ER sounds like "letter," and the long version is good for monosyllabic words like "fir." One final suggestion is that you may want to add a pause of 30–50 msec. between words, when creating sentences, and a pause of 100–200 msec. between clauses.

Note: Every utterance must be followed by a pause in order to make the chip stop speaking the last allophone.

TABLE 1: THE ALLOPHONE DICTIONARY

NUMBERS

zero	ZZ YR OW
one, won	WW SX ZX NN1
two, to, too	TT2 UW2
three	TH RR1 IY
four, for, fore	FF FF OR
five	FF FF AY VV
six	SS SS IH IH PA3 KK2 SS
seven	SS SS EH EH VV IH NN1
eight, ate	EY PA3 TT2
nine	NN1 AA AY NN1
ten	TT2 EH EH NN1
eleven	IH LL EH EH VV IH NN1
twelve	TT2 WH EH EH LL VV
thirteen	TH ER1 PA2 PA3 TT2 IY NN1
fourteen	FF OR PA2 PA3 TT2 IY NN1
fifteen	FF IH FF PA2 PA3 TT2 IY NN1
sixteen	SS SS IH PA3 KK2 SS PA2 PA3 TT2 IY NN1
seventeen	SS SS EH VV TH NN1 PA2 PA3 TT2 IY NN1
eighteen	EY PA2 PA3 TT2 IY NN1
nineteen	NN1 AY NN1 PA2 PA3 TT2 IY NN1
twenty	TT2 WH EH EH NN1 PA2 PA3 TT2 IY
thirty	TH ER2 PA2 PA3 TT2 IY
forty	FF OR PA3 TT2 IY
fifty	FF FF IH FF FF PA2 PA3 TT2 IY
sixty	SS SS IH PA3 KK2 SS PA2 PA3 TT2 IY
seventy	SS SS EH VV IH NN1 PA2 PA3 TT2 IY
eighty	EY PA3 TT2 IY
ninety	NN1 AY NN1 PA3 TT2 IY
hundred	HH2 AX AX NN1 PA2 DD2 RR2 IH IH PA1 DD1
thousand	TH AA AW ZZ TH PA1 PA1 NN1 DD1
million	MM IH IH LL YY1 AX NN1

DAY OF THE WEEK:

Sunday	SS SS AX AX NN1 PA2 DD2 EY
Monday	MM AX AX NN1 PA2 DD2 EY
Tuesday	TT2 UW2 ZZ PA2 DD2 EY
Wednesday	WW EH EH NN1 ZZ PA2 DD2 EY
Thursday	TH ER2 ZZ PA2 DD2 EY
Friday	FF RR2 AY PA2 DD2 EY
Saturday	SS SS AE PA3 TT2 PA2 DD2 EY

MONTHS:

January	JH AE AE NN1 YY2 XR IY
February	FF EH EH PA2 BR RR2 UW2 XR IY
March	MM AR PA3 CH
April	EY PA3 PP RR2 IH IH LL
May	MM EY
June	JH UW2 NN1
July	JH UW1 LL AY
August	AO AO PA2 GG2 AX SS PA3 TT1
September	SS SS EH PA3 PP PA3 TT2 EH EH PA1 BB2 ER1
October	AA PA2 KK2 PA3 TT2 OW PA1 BB2 ER1
November	NN2 OW VV EH EH MM PA1 BB2 ER1
December	DD2 IY SS SS EH EH MM PA1 BB2 ER1

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ALLOPHONE DICTIONARY (Continued)

LETTERS:

A	EY
B	BB2 IY
C	SS SS IY
D	DD2 IY
E	IY
F	EH EH FF FF
G	JH IY
H	EY PA2 PA3 CH
I	AA AY
J	JH EH EY
K	KK1 EH EY
L	EH EH EL
M	EH EH EM
N	EH EH NN1
O	OW
P	PP IY
Q	KK1 YY1 UW2
R	AR
S	EH EH SS SS
T	TT2 IY
U	YY1 UW2
V	VV IY
W	DD2 AX PA2 BB2 YY1 UW2
X	EH EH PA3 KK2 SS SS
Y	WW AY
Z	ZZ IY

DICTIONARY

alarm	AX LL AR MM
bathe	BB2 EH DH2
bather	BB2 EY DH2 ER1
bathing	BB2 EY DH2 IH NG
beer	BB2 YR
bread	BB1 RR2 EH EH PA1 DD1
by	BB2 AA AY
calendar	KK1 AE AE LL EH NN1 PA2 DD2 ER1
clock	KK1 LL AA AA PA3 KK2
clown	KK1 LL AW NN1
check	CH EH EH PA3 KK2
checked	CH EH EH PA3 KK2 PA2 TT2
checker	CH EH EH PA3 KK1 ER1
checkers	CH EH EH PA3 KK1 ER1 ZZ
checking	CH EH EH PA3 KK1 IH NG
checks	CH EH EH PA3 KK1 SS
cognitive	KK3 AA AA GG3 NN1 IH PA3 TT2 IH VV
collide	KK3 AX LL AY DD1
computer	KK1 AX MM PP1 YY1 UW1 TT2 ER
cookie	KK3 UH KK1 IY
coop	KK3 UW2 PA3 PP
correct	KK1 ER2 EH EH PA2 KK2 PA2 TT1
corrected	KK1 ER2 EH EH PA2 KK2 PA2 TT2 IH PA2 DD1
correcting	KK1 ER2 EH EH PA2 KK2 PA2 TT2 IH NG
corrects	KK1 ER2 EH EH PA2 KK2 PA2 TT1 SS
crown	KK1 RR2 AW NN1
date	DD2 EY PA3 TT2
daughter	DD2 AO TT2 ER1
day	DD2 EH EY
divided	DD2 IH VV AY PA2 DD2 IH PA2 DD1
emotional	IY MM OW SH AX NN1 AX EL
engage	EH EH PA1 NN1 GG1 EY PA2 JH
engagement	EH EH PA1 NN1 GG1 EY PA2 JH MM EH EH NN1 PA2 PA3 TT2
engages	EH EH PA1 NN1 GG1 EY PA2 JH IH ZZ
engaging	EH EH PA1 NN1 GG1 EY PA2 JH IH NG
enrage	EH NN1 RR1 EY PA2 JH
enraged	EH NN1 RR1 EY PA2 JH PA2 DD1
enrages	EH NN1 RR1 EY PA2 JH IH ZZ
enraging	EH NN1 RR1 EY PA2 JH IH NG
escape	EH SS SS PA3 KK1 PA2 PA3 PP
escaped	EH SS SS PA3 KK1 PA2 PA3 PP PA2 TT2
escapes	EH SS SS PA3 KK1 PA2 PA3 PP SS
escaping	EH SS SS PA3 KK1 PA2 PA3 PP IH NG
equal	IY PA2 PA3 KK3 WH AX EL
equals	IH PA2 PA3 KK3 WH AX EL ZZ
error	EH XR OR
extent	EH KK1 SS TT2 EH EH NN1 TT2
fir	FF ER2
freeze	FF FF RR1 IY ZZ
freezer	FF FF RR1 IY ZZ ER1
freezers	FF FF RR1 IY ZZ ER1 ZZ
freezing	FF FF RR1 IY ZZ IH NG
frozen	FF FF RR1 OW ZZ EH NN1
gauge	GG1 EY PA2 JH
gauged	GG1 EY PA2 JH PA2 DD1
gauges	GG1 EY PA2 JH IH ZZ
gauging	GG1 EY PA2 JH IH NG
hello	HH EH LL AX OW
hour	AW ER1
infinitive	IH NN1 FF FF IH IH NN1 IH PA2 PA3 TT2 IH VV
intrigue	IH NN1 PA3 TT2 RR2 IY PA1 GG3
intrigued	IH NN1 PA3 TT2 RR2 IY PA1 GG3 PA2 DD1
intrigues	IH NN1 PA3 TT2 RR2 IY PA1 GG3 ZZ
intriguing	IH NN1 PA3 TT2 RR2 IY PA1 GG3 IH NG
investigate	IH IH NN1 VV EH EH SS PA2 PA3 TT2 IH PA1 GG1 EY PA2 TT2
investigated	IH IH NN1 VV EH EH SS PA2 PA3 TT2 IH PA1 GG1 EY PA2 TT2 IH PA2 DD1
investigater	IH IH NN1 VV EH EH SS PA2 PA3 TT2 IH PA1 GG1 EY PA2 TT2 ER1
investigaters	IH IH NN1 VV EH EH SS PA2 PA3 TT2 IH PA1 GG1 EY PA2 TT2 ER1 ZZ
investigates	IH IH NN1 VV EH EH SS PA2 PA3 TT2 IH PA1 GG1 EY PA2 TT1 SS
investigating	EH EH NN1 VV EH EH SS PA2 PA3 TT2 IH PA1 GG1 EY PA2 TT2 IH NG
key	KK1 IY
legislate	LL EH EH PA2 JH JH SS SS LL EY PA2 PA3 TT2
legislated	LL EH EH PA2 JH JH SS SS LL EY PA2 PA3 TT2 IH DD1
legislates	LL EH EH PA2 JH JH SS SS LL EY PA2 PA3 TT1 SS

ALLOPHONE DICTIONARY
DICTIONARY (Continued)

legislating	LL EH EH PA2 JH JH SS SS LL EY PA2 PA3 TT 2 IH NG
legislature	LL EH EH PA2 JH JH SS SS LL EY PA2 PA3 CH ER1
letter	LL EH EH PA3 TT2 ER1
litter	LL IH IH PA3 TT2 ER1
little	LL IH IH PA3 TT2 EL
memory	MM EH EH MM ER2 IY
memories	MM EH EH MM ER2 IY ZZ
minute	MM 1H NN1 IH PA3 TT2
month	MM AX NN1 TH
nip	NN1 IH IH PA2 PA3 PP
nipped	NN2 IH IH PA2 PA3 PP PA3 TT2
nipping	NN1 IH IH PA2 PA3 PP IH NG
nips	NN1 IH IH PA2 PA3 PP SS
no	NN2 AX OW
physical	FF FF IH ZZ IH PA3 KK1 AX EL
pin	PP IH IH NN1
pinned	PP IH IH NN1 PA2 DD1
pinning	PP IH IH NN1 IH NG1
pins	PP IH IH NN1 ZZ
pledge	PP LL EH FH PA3 JH
pledged	PP LL EH EH PA3 JH PA2 DD1
pledges	PP LL EH EH PA3 JH IH ZZ
pledging	PP LL EH EH PA3 JH IH NG
plus	PP LL AX AX SS SS
ray	RR1 EH EY
rays	RR1 EH EY ZZ
ready	RR1 EH EH PA1 DD2 IY
red	RR1 EH FH PA1 DD1
robot	RR1 OW PA2 BB2 AA PA3 TT2
robots	RR1 OW PA2 BB2 AA PA3 TT1 SS
score	SS SS PA3 KK3 OR
second	SS SS EH PA3 KK1 IH NN1 PA2 DD1
sensitive	SS SS EH EH NN1 SS SS IH PA2 PA3 TT2 IH VV
sensitivity	SS SS EH EH NN1 SS SS IH PA2 PA3 TT2 IH VV IH PA2 PA3 TT2 IY
sincere	SS SS IH IH NN1 SS SS YR
sincerely	SS SS IH IH NN1 SS SS YR LL IY
sincerity	SS SS IH IH NN1 SS SS EH EH RR1 IH PA2 PA3 TT2 IY
sister	SS SS IH IH SS PA3 TT2 ER1
speak	SS SS PA3 IY PA3 KK2
spell	SS SS PA3 PP EH EH EL
spelled	SS SS PA3 PP EH EH EL PA3 DD1
speller	SS SS PA3 PP EH EH EL ER2
spellers	SS SS PA3 PP EH EH EL ER2 ZZ
spelling	SS SS PA3 PP EH EH EL IH NG
spells	SS SS PA3 PP EH EH EL ZZ
start	SS SS PA3 TT2 AR PA3 TT2
started	SS SS PA3 TT2 AR PA3 TT2 IH PA1 DD2
starter	SS SS PA3 TT2 AR PA3 TT2 ER1
starting	SS SS PP3 TT2 AR PA3 TT2 IH NG
starts	SS SS PP3 TT2 AR PA3 TT1 SS
stop	SS SS PA3 TT1 AA AA PA3 PP
stopped	SS SS PA3 TT1 AA AA PA3 PP PA3 TT2
stopper	SS SS PA3 TT1 AA AA PA3 PP ER1
stopping	SS SS PA3 TT1 AA AA PA3 PP IH NG
stops	SS SS PA3 TT1 AA AA PA3 PP SS
subject (noun)	SS SS AX AX PA2 BB1 PA2 JH EH PA3 KK2 PA3 TT2
subject (verb)	SS SS AX PA2 BB1 PA2 JH EH EH PA3 KK2 PA3 TT2
sweat	SS SS WW EH EH PA3 TT2
sweated	SS SS WW EH EH PA3 TT2 IH PA3 DD1
sweater	SS SS WW EH EH PA3 TT2 ER1
sweaters	SS SS WW EH EH PA3 TT2 ER1 ZZ
sweating	SS SS WW EH EH PA3 TT2 IH NG
sweats	SS SS WW EH EH PA3 TT2 SS
switch	SS SS WH IH IH PA3 CH
switched	SS SS WH IH IH PA3 CH PA3 TT2
switches	SS SS WH IH IH PA3 CH IH ZZ2
switching	SS SS WH IH IH PA3 CH IH NG2
system	SS SS IH IH SS SS PA3 TT2 EH MM
systems	SS SS IH IH SS SS PA3 TT2 EH MM ZZ
talk	TT2 AO AO PA2 KK2
talked	TT2 AO AO PA3 KK2 PA3 TT2
talker	TT2 AO AO PA3 KK1 ER1
talkers	TT2 AO AO PA3 KK1 ER1 ZZ
talking	TT2 AO AO PA3 KK1 IH NG
talks	TT2 AO AO PA2 KK2 SS
thread	TH RR1 EH EH PA2 DD1
threaded	TH RR1 EH EH PA2 DD2 IH PA2 DD1
threader	TH RR1 EH EH PA2 DD2 ER1
threaders	TH RR1 EH EH PA2 DD2 ER1 ZZ
threading	TH RR1 EH EH PA2 DD2 IH NG
threads	TH RR1 EH EH PA2 DD2 ZZ
then	DH1 EH EH NN1
time	TT2 AA AY MM
times	TT2 AA AY MM ZZ
uncle	AX NG PA3 KK3 EL
whale	WW EY EL
whaler	WW EY LL ER1
whalers	WW EY LL ER1 ZZ
whales	WW EY EL ZZ
whaling	WW EY LL TH NG
year	YY2 YR
yes	YYS EH EH SS SS

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TABLE 2—EXAMPLES OF SPELLING IRREGULARITIES

	Same sound represented by different letters	Different sounds represented by the same letters
Vowels	mEAt fEEt pEte pEOple pennY	vEIn forEIgn dEIsm dEIcer gEIsha
Consonants	SHip tenSIon preCIous naTIon	althouGH GHastly couGH hiccouGH

TABLE 3—CONSONANT PHONEMES OF ENGLISH

		LABIAL	LABIO-DENTAL	INTER-DENTAL	ALVEO-LAR	PALATAL	VELAR	GLOTTAL
Stops:	Voiceless Voiced	PP BB			TT DD		KK GG	
Fricatives:	Voiceless Voiced	WH	FF VV	TH DH	SS ZZ	SH ZH*		HH
Affricates:	Voiceless Voiced					CH JH		
Nasals	Voiced	MM			NN		NG*	
Resonants	Voiced	WW			RR,LL	YY		

These do not occur in word-initial position in English.

Labial: Upper and Lower Lips Touch or Approximate
Labio-Dental: Upper Teeth and Lower Lip Touch
Inter-Dental: Tongue Between Teeth
Alveolar: Tip of Tongue Touches or Approximates Alveolar Ridge (just behind upper teeth)
Palatal: Body of Tongue Approximates Palate (roof of mouth)
Velar: Body of Tongue Touches Velum (posterior portion of roof of mouth)
Glottal: Glottis (opening between vocal cords)

TABLE 4—VOWEL PHONEMES OF ENGLISH

	FRONT	CENTRAL	BACK
High	YR IY IH*		UW# UH*#
Mid	EY EH* XR	ER AX*	OW# OY#
Low	AE*	AW# AY AR AA*	AO*# OR#

*SHORT VOWELS
#ROUNDED VOWELS

TABLE 5—GUIDELINES FOR USING THE ALLOPHONES

Silence

PA1	(10 ms)	—before BB, DD, GG and JH
PA2	(30 ms)	—before BB, DD, GG, and JH
PA3	(50 ms)	—before PP, TT, KK, and CH, and between words
PA4	(100 ms)	—between clauses and sentences
PA5	(200 ms)	—between clauses and sentences

Short Vowels

*/IH/	—sitting, stranded
*/EH/	—extent, gentlemen
*/AE/	—extract, acting
*/UH/	—cookie, full
*/AO/	—talking, song
*/AX/	—lapel, instruct
*/AA/	—pottery, cotton

Long Vowels

/IY/	—treat, people, penny
/EY/	—great, statment, tray
/AY/	—Kite, sky, mighty
/OY/	—noise, toy, voice
/UW1/	—after clusters with YY; computer
/UW2/	—in monosyllabic words: two, food
/OW/	—zone, close, snow
/AW/	—sound, mouse, down
/EL/	—little, angle, gentlemen

R-Colored Vowels

/ER1/	—letter, furniture, interrupt
/ER2/	—monosyllables: bird, fern, burn
/OR/	—fortune, adorn, store
/AR/	—farm, alarm, garment
/YR/	—hear, earring, irresponsible
/XR/	—hair, declare, stare

Resonants

/WW/	—we, warrant, linguist
/RR1/	—initial position: read, write, x-ray
/RR2/	—initial clusters: brown, crane, grease
/LL/	—like, hello, steel
/YY1/	—clusters: cute, beauty, yarn, yo-yo
/YY2/	—initial position: yes, yarn, yo-yo

Voiced Fricatives

/VV/	—vest, prove, even
/DH1/	—word-initial position: this, then, they
/DH2/	—word-final and between vowels: bathe, bathing
/ZZ/	—zoo, phase
/ZH/	—beige, pleasure

Voiceless Fricatives

*/FF/	—) These may be doubled for initial position and used singly in final position
*/TH/	—)
*/SS/	—)
/SH/	—shirt, leash, nation
/HH1/	—before front vowels, RY, IY, IH EY, EH, XR, AE
/HH2/	—before back vowels: UW, UH, OW, OY, AO, OR, AR
/WH/	—white, whim, twenty

Voiced Stops

/BB1/	—final position: rib; between vowels: fibber; —in clusters: bleed, brown
/BB2/	—initial position before a vowel: beast
/DD1/	—final position: played, end
/DD2/	—initial position: down; clusters: drain
/GG1/	—before high front vowels: YR, IY, IH, EY, EH, XR
/GG2/	—before high back vowels: UW, UH, OW, OY, AX; and —clusters; green, glue
/GG3/	—before low vowels: AE, AW, AY, AR, AA, AO, OR, ER; and —medial clusters: anger; and final position: peg

Voiceless Stops

/PP/	—pleasure, ample, trip
/TT1/	—final clusters before SS: tests, its
/TT2/	—all other positions: test, street
/KK1/	—before front vowels: YR, IY, IH, EY, EH, XR, AY, AE, ER, AX; —initial clusters: cute, clown, scream
/KK2/	—final position: speak; final clusters: task
/KK3/	—before back vowels: UW, UH, OW, OY, OR, AR, AQ; —initial clusters: crane, quick, clown, scream

Affricates

/CH/	—church, feature
/JH/	—judge, injure

Nasal

/MM/	—milk, alarm, ample
/NN/	—before front and central vowels: YR, IY, IH, EY, EH, XR, AE, ER, AX, AW, AY, UW; final clusters: earn
/NN2/	—before back vowels: UH, OW, OY, CR, AR, AA
/NG/	—string, anger

*These allophones can be doubled.

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TABLE 6—ALLOPHONE ADDRESS TABLE

OCTAL ADDRESS	ALLOPHONE	SAMPLE WORD	DURATION
000	PA1	PAUSE	10MS
001	PA2	PAUSE	30MS
002	PA3	PAUSE	50MS
003	PA4	PAUSE	100MS
004	PA5	PAUSE	200MS
005	/OY/	Boy	420MS
006	/AY/	Sky	260MS
007	/EH/	End	70Ms
010	/KK3/	Comb	120MS
011	/PP/	Pow	210MS
012	/JH/	Dodge	140MS
013	/NN1/	Thin	140MS
014	/IH/	Sit	70MS
015	/TT2/	to	140MS
016	/RR1/	Rural	170MS
017	/AX/	Succeed	70MS
020	/MM/	Milk	180MS
021	/TT1/	Part	100MS
022	/DH1/	They	290MS
023	/IY/	See	250MS
024	/EY/	Beige	280MS
025	/DD1/	Could	70MS
026	/UW1/	To	100MS
027	/AO/	Aught	100MS
030	/AA/	Hot	100MS
031	/YY2/	Yes	180MS
032	/AE/	Hat	120MS
033	/HH1/	He	130MS
034	/BB1	Business	80MS
035	/TH/	Thin	180MS
036	/UH/	Book	100MS
037	/UW2/	Food	260MS
040	/AW/	Out	370MS
041	/DD2/	Do	160MS
042	/GG3/	Wig	140MS
043	/VV/	Vest	190MS
044	/GG1/	Got	80MS
045	/SH/	Ship	160MS
046	/ZH/	Azure	190MS
047	/RR2/	Brain	120MS
050	/FF/	Food	150MS
051	/KK2/	Sky	190MS
052	/KK1/	Can't	160MS
053	/ZZ/	Zoo	210MS
054	/NG/	Anchor	220MS
055	/LL/	Lake	110MS
056	/WW/	Wool	180MS
057	/XR/	Repair	360MS
060	/WH/	Whig	200MS
061	/YY1/	yes	130MS
062	/CH/	Church	190MS
063	/ER1/	Fir	160MS
064	/ER2/	Fir	300MS
065	/OW/	Beau	240MS
066	/DH2/	They	240MS
067	/SS/	Vest	90MS
070	/NN2/	No	190MS
071	/HH2/	Hoe	180MS
072	/OR/	Store	330MS
073	/AR/	Alarm	290MS
074	/YR/	Clear	350MS
075	/GG2/	Guest	40MS
076	/EL/	Saddle	190MS
077	/BB2/	Business	50MS

PROGRAMMABLE SOUND GENERATOR

AY-3-8910A
276-1787

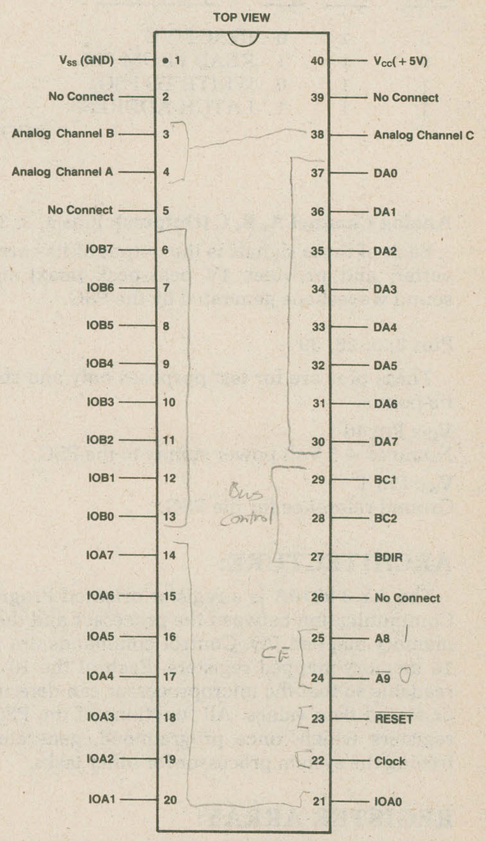
GENERAL DESCRIPTION

The AY-3-8910A Programable Sound Generator (PSG) is an LSI circuit which can produce a wide variety of complex sounds under software control. The AY-3-8910A is manufactured in the Microelectronics N-Channel Ion Implant Process. Operation requires a single +5V power supply, a TTL compatible clock, and a microprocessor controller.

The PSG is easily interfaced to any bus-oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signaling, and home computer usage. In order to generate sound effects while allowing the processor to perform other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one component is satisfied by the three independently controllable analog sound-output channels available in the PSG. These analog sound-output channels can each provide 4 bits of logarithmic digital-to-analog conversion, greatly enhancing the dynamic range of the sounds produced.

All circuit control signals are digital in nature and may be provided directly by a miroprocessor/microcomputer. Therefore, one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction.

PIN CONNECTION



FEATURES

- Full software control of sound generation
- Interfaces to most 8-bit and 16-bit microprocessors
- Three independently programmable analog outputs
- One or two 8-bit I/O ports
- Full 0° to 70°C operation

ABSOLUTE MAXIMUM RATING

V_{CC} and all other Input/Output
Voltages with Respect to V_{SS} .... −0.3V to +8.0V
Storage Temperature .... −55°C to +150°C
Operating Temperature ....0°C to +70°C

PIN FUNCTIONS

DA7–DA0 (Input/Output/High Impedance)
Data/Address Bits 7–0: Pins 30–37

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG, and to receive data from the PSG. In the address mode, DA3–DA0 select the internal register address ($0–17_8$) and DA7–DA4 in conjunction with address inputs $\overline{A9}$ and A8, form the chip select function. When the high order address bits are "incorrect," the bidirectional buffers are forced to a high impedance state.

$\overline{\text{Address 9}}$, Address 8
A8 (input): Pin 25
$\overline{A9}$ (input): Pin 24

High order address bits $\overline{A9}$ and A8 are fixed to recognize a "01" code. They may be left unconnected, as each is provided with either an on-chip pull-down ($\overline{A9}$) or pull-up (A8) resistor. In noisy environments, however, it is recommended the $\overline{A9}$ and A8 be tied to external ground and +5V respectively, if they are not to be used.

$\overline{\text{RESET}}$ (Input): Pin 23

For initialization/power-on purposes, applying a low level input to the $\overline{\text{RESET}}$ pin will reset all registers to 0_8. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up register.

CLOCK (Input): Pin 22

This TTL compatible input supplies the timing reference for the Tone, Noise, and Envelope Generators.

BDIR, BC2, BC1 (Inputs): Pins 27, 28, 29

BUS Direction, BUS Control 2, Bus Control 1

These bus control signals are generated directly by a microprocessor to control all bus operations internal and external to the PSG.

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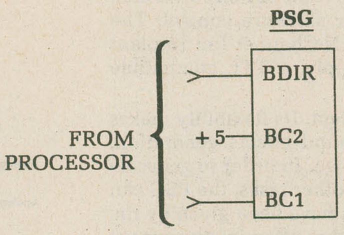
BDIR	BC2	BC1	PSG FUNCTION
Rd 0	1	0	INACTIVE.
0	1	1	READ FROM PSG.
1	1	0	WRITE TO PSG.
WR 1	1	1	LATCH ADDRESS.



Analog Channel A, B, C (Outputs): Pins 4, 3, 38

Each of these signals is the output of its corresponding digital to analog converter, and provides 1V peak-peak (max) signal representing the complex sound waveshape generated by the PSG.

Pins 2, 5, 26, 39

These pins are for test purposes only and should be left open. Do not use as tie-points.

V_{CC}: Pin 40
Nominal +5 Volt power supply to the PSG.

V_{SS}: Pin 1
Ground reference for the PSG.

ARCHITECTURE:

The AY-3-8910A is a register oriented Programable Sound Generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, if necessary, present states or stored data values. All functions of the PSG are controlled through the 16 registers which, once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

REGISTER ARRAY:

The principal element of the PSG is the array of 16 read/write control registers. These 16 registers look to the CPU as a block of memory and, as such, occupy a 16-word block out of 1,024 possible addresses. The 10 address bits (8 bits on the common data/address bus, and 2 separate address bits) are decoded as follows:

$\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	0	0	0	0
THROUGH									
0	1	0	0	0	0	1	1	1	1
HIGH ORDER (Chip Select)						LOW ORDER (Register No.)			

The four low order address bits select one of the 16 registers ($R0–R17_8$). The six high order address bits function as chip selects to control the tri-state bidirectional buffers (when the high order address bits are incorrect, the bidirectional buffers are forced to a high impedance state). High order address bits $\overline{A9}$, A8 are fixed in the PSG design to recognize a "01" code; high order address bits DA7–DA4 are programmed to recognize only a "0000" code. All addresses are latched internally. This internally latched address is updated and modified on every latch address signal presented to the PSG via the BDIR, BC2, and BC1 inputs. A latched address will remain valid until the receipt of a new address, enabling multiple reads and writes of the same register contents without the need for redundant re-addressing.

Conditioning of the Register Address Latch/Decoder and the Bidirectional Buffers to recognize the bus function required (Inactive, Latch Address, Write Data), is accomplished by the Bus Control Decode block.

SOUND GENERATING BLOCKS:

The basic blocks in the PSG which produce the programmed sounds include:

Tone Generators	Produce the basic square wave tone frequencies for each channel (A, B, C).
Noise Generator	Produces a pulse width modulated pseudo-random square wave output.
Mixers	Combine the outputs of the Tone Generators and the Noise Generator; per channel (A, B, C).
Envelope Generator	Produces an envelope pattern which can be used to amplitude modulate the output of each Mixer.
Amplitude Control	Provides the D/A Converters with either a fixed or variable amplitude pattern. Fixed amplitude is under direct CPU control. Variable amplitude is accomplished via the output of the Envelope Generator.
D/A Converters	The three D/A Converters each produce a 16 level (max) output signal as determined by the Amplitude Control.

OPERATION

Since all PSG functions are processor controlled by writing to the internal registers, a detailed description of the PSG operation may best be accomplished by relating each PSG function to control of the corresponding register. The function of creating or programming a specific sound effect logically follows the control sequence listed:

Operation	Registers	Function
Tone Generator Control	R0–R5	Program tone periods
Noise Generator Control	R6	Program noise period
Mixer Control	R7	Enable tone and/or noise on selected channels
Amplitude Control	R10–R12	Select fixed or variable (envelope) amplitudes
Envelope Generator Control	R13–R15	Program envelope period and select envelope pattern

Tone Generator Control

(Registers R0, R1, R2, R3, R4, R5)

The frequency of each square wave generated by the three Tone Generators (one each for Channels A, B, and C) is obtained by first dividing the input clock by 16 then by further dividing the result by the programmed 12-bit Tone Period value. Each 12-bit tone period value is obtained by combining the contents of the respective Coarse and Fine Tune registers, as illustrated:

Coarse Tune Register	Channel	Fine Tune Register
R1	A	R0
R3	B	R2
R5	C	R4

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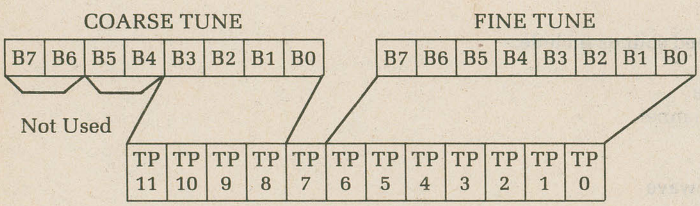


12-bit Tone Period (TP) to Tone Generator

The period of the output of the tone generator is therefore determined by:

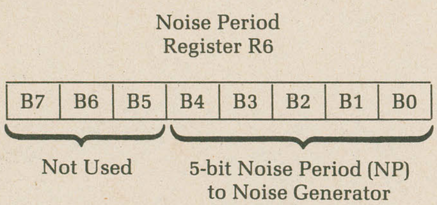
16 × TP × P where P = the period of the input clock.

NOTE: If the Coarse and Fine Tune registers are both set to 000_8, the resulting period will be minimum, i.e., the generated tone period will be as if the Coarse Tune register was set to 000_8 and the Fine Tune register set to 001_8.

Noise Generator Control

(Register R6)

The frequency of the noise source is obtained by dividing the input clock by 16, then by further dividing the result by the programmed 5-bit Noise Period value. This 5-bit value consists of the lower 5 bits (B4–B0) of register R6, as illustrated:



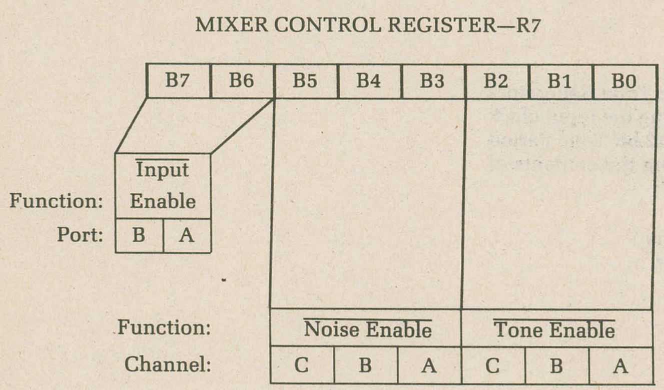
Mixer Control—I/O Enable

(Register R7)

Register R7 is a multi-function $\overline{\text{ENABLE}}$ register which controls the three Noise/Tone Mixers.

The Mixers, previously described, combine the noise and tone frequencies for each of the three channels. The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5–B0 of register R7, as illustrated.

The direction (input or output) of the general purpose I/O ports (I/OA and I/OB) is determined by the state of bits B7 and B6 of R7, as illustrated.



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NOISE ENABLE TRUTH TABLE

R7 Bits B5	B4	B2	Noise Enabled on Channel		
0	0	0	C	B	A
0	0	1	C	B	—
0	1	0	C	—	A
0	1	1	C	—	—
1	0	0	—	B	A
1	0	1	—	B	—
1	1	0	—	—	A
1	1	1	—	—	—

TONE ENABLE TRUTH TABLE

R7 Bits B2	B1	B0	Tone Enabled on Channel		
0	0	0	C	B	A
0	0	1	C	B	—
0	1	0	C	—	A
0	1	1	C	—	—
1	0	0	—	B	A
1	0	1	—	B	—
1	1	0	—	—	A
1	1	1	—	—	—

I/O PORT TRUTH TABLE

R7 Bits B7	B6	I/O Port Status I/OB	I/OA
0	0	Input	Input
0	1	Input	Output
1	0	Output	Input
1	1	Output	Output

NOTE: Disabling noise and tone does *not* turn off a channel. Turning a channel off can only be accomplished by writing all zeros into the corresponding Amplitude Control Register.

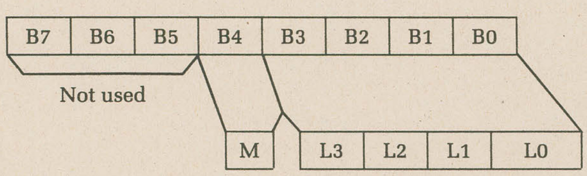
Amplitude Control

(Registers R10, R11, R12)

The amplitude of the signals generated by each of the three D/A Converters (one each for Channels A, B, and C) is determined by the content of the lower bits (B4–B0) of registers R10, R11, and R12 as illustrated.

These five bits consists of a 1-bit mode select ("M" bit) and a 4-bit "fixed" amplitude level (L3–L0). When the M bit is low, the output level of the analog channel is defined by the 4-bit "fixed" amplitude level of the Amplitude Control Register. This amplitude level is fixed in the sense that the amplitude level is under direct control of the system processor. When the M bit is high, the output level of the analog channel is defined by the 4-bits of the Envelope Generator (bits E3–E0). The amplitude mode bit can also be thought of as an "envelope enable" bit.

Amplitude Control Register	Channel
R10	A
R11	B
R12	C



Amplitude Mode	4 bit fixed Amplitude Level				
0	0	0	0	0	Amplitude Defined By L0–L3
'	'			'	
'	'			'	
'	'			'	
0	1	1	1	1	
1	X	X	X	X	Amplitude Defined By E0–E3

Envelope Generator Control

To accomplish the generation of complex envelope patterns, two independent methods of control are provided: first, it is possible to vary the frequency of the envelope using registers R13 and R14; second, the relative shape and cycle pattern of the envelope can be varied using register R15. The following paragraphs explain the details of the envelope control functions, describing first the envelope period control and then the envelope shape/cycle control. (See Figures 1 and 2).

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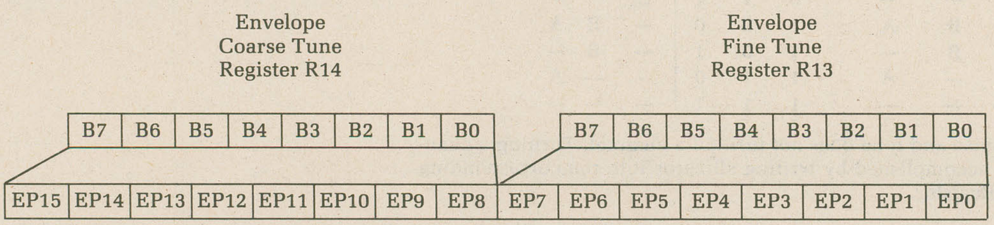
Envelope Period Control

(Registers R13, R14)

The frequency of the envelope is obtained by first dividing the input clock by 256, then by further dividing the result by the programmed 16-bit Envelope Period value. This 16-bit value is obtained by combining the contents of the Envelope Coarse and Fine Tune registers, as illustrated:



16-bit Envelope Period (EP) to Envelope Generator
Thus the envelope period is given by:
256 x EP x P   Where P = period of input clock

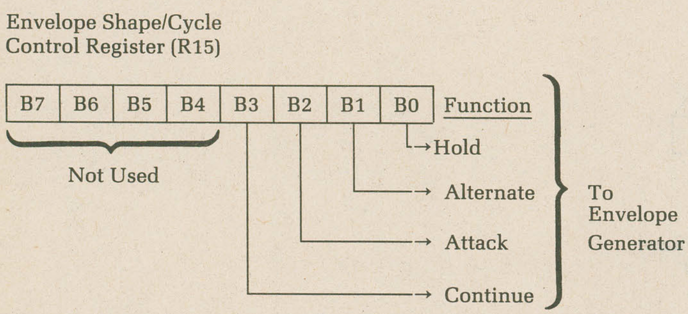
NOTE: If the Coarse and Fine Tune registers are both set to 000_8, the resulting period will be minimum, i.e., the generated tone period will be as if the Coarse Tune register was set to 000_8 and the Fine Tune register set to 001_8.

Envelope Shape/Cycle Control

(Register R15)

The Envelope Generator further divides the envelope period by 16, producing a 16-state per cycle envelope pattern as defined by the 4-bit counter output, E3, E2, E1 and E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern of the 4-bit counter. (See Figures 4 and 5).

This envelope shape/cycle control is contained in the lower 4 bits (B3–B0) of register R15. Each of these 4 bits controls a function in the envelope generator, as illustrated:



Bit 0:	HOLD	When this is set high (logic 1) the envelope is limited to one cycle, the value of the envelope at the end of the cycle being held.
Bit 1:	ALTERNATE	When set high (logic 1) the envelope counter reverses direction at end of each cycle (i.e. performs as an up/down counter).
Bit 2:	ATTACK	When set high (logic 1) the envelope counter will count up (attack). When set low (logic 0) the counter will count down (decay).
Bit 3:	CONTINUE	When set high (logic 1) the cycle pattern will be defined by the HOLD bit. When set low (logic 0) the envelope counter will reset to 0000 after one cycle, and hold that value.

D/A CONVERTER OPERATION

Since the primary use of the PSG is to produce sound for the non-linear amplitude detection mechanism of the human ear, the D/A conversion is performed in logarithmic steps with a normalized voltage range from 0 to 1 volt. The specific amplitude control of each of the three D/A Converters is accomplished by the three sets of 4 bit outputs of the Amplitude Control block, while the Mixer outputs provide the base signal frequency (Noise and/or Tone). (See Fig. 3).

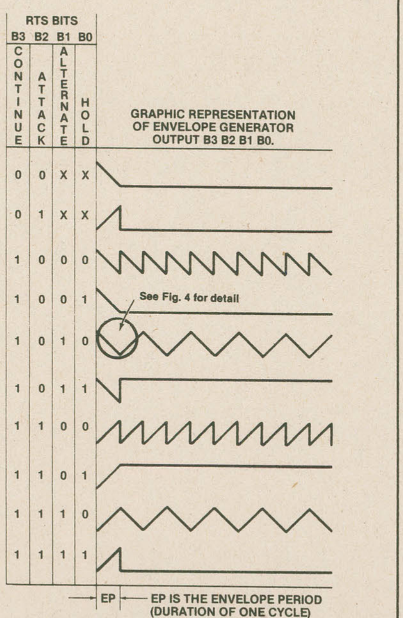


FIG. 1 ENVELOPE SHAPE/CYCLE OPERATION

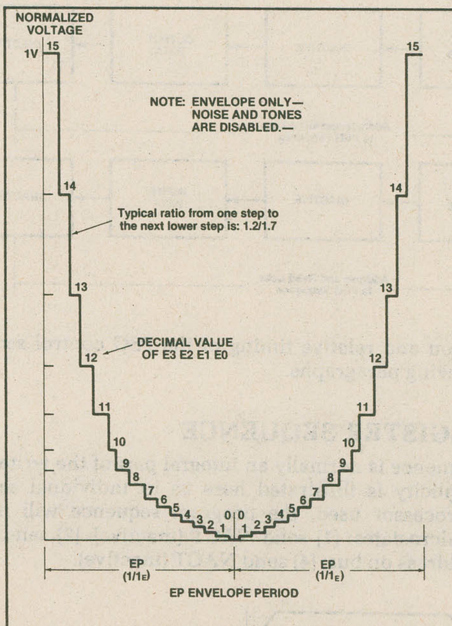


FIG. 3 D/A CONVERTER OUTPUT

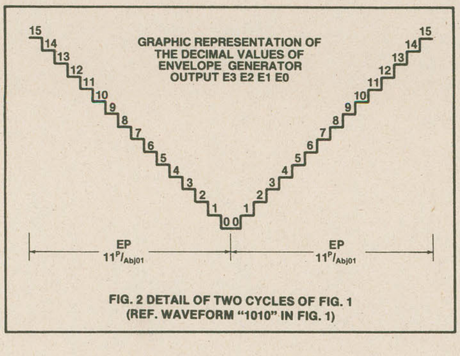


FIG. 2 DETAIL OF TWO CYCLES OF FIG. 1 (REF. WAVEFORM "1010" IN FIG. 1)

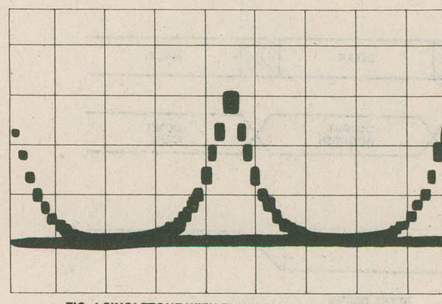


FIG. 4 SINGLETONE WITH ENVELOPE SHAPE/CYCLE PATTERN 1010

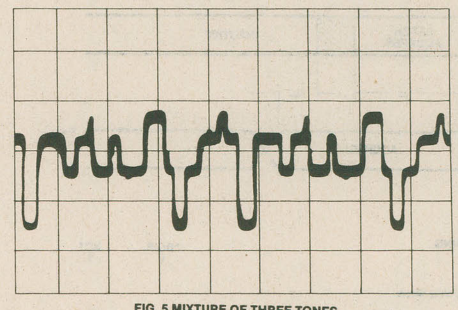
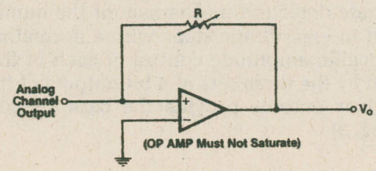


FIG. 5 MIXTURE OF THREE TONES WITH FIXED AMPLITUDES

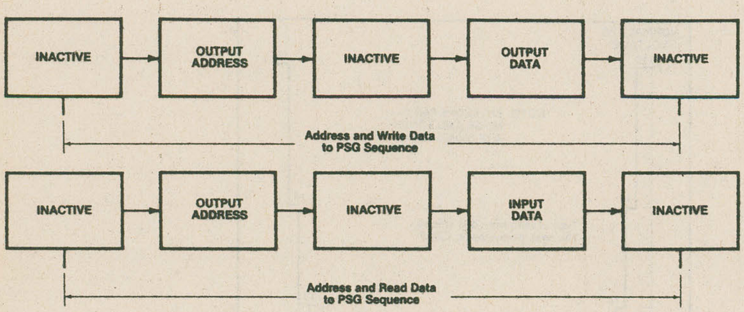
AY-3-8910A 276-1787



ANALOG CHANNEL OUTPUT TEST CIRCUIT

STATE TIMING

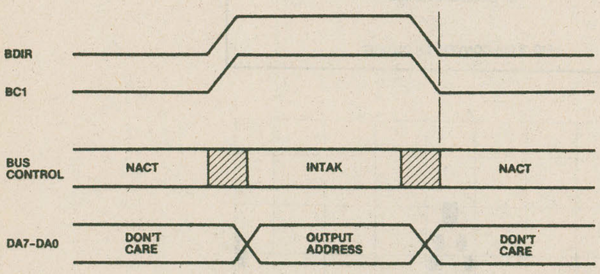
While the state flow for many microprocessors can be somewhat involved for certain operations, the sequence of events necessary to control the PSG is simple and straightforward. Each of the three major state sequences (Latch Address, Write to PSG, and Read from PSG) consists of several operations (indicated below by rectangular blocks), defined by the pattern of bus control signals (BDIR, BC1).

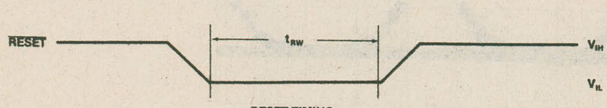


The functional operation and relative timing of the PSG control sequences are described in the following paragraphs.

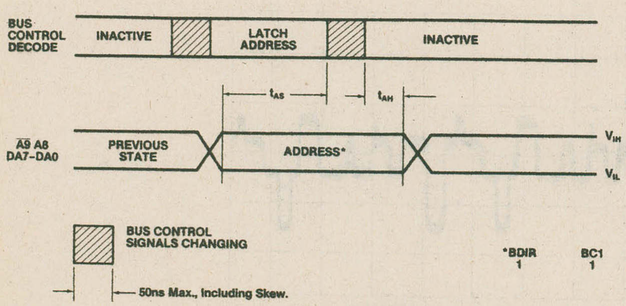
ADDRESS PSG REGISTER SEQUENCE

The Latch Address sequence is normally an integral part of the write or read sequences, but for simplicity is illustrated here as in individual sequence. Depending upon the processor used, the program sequence will normally require four principal microstates: (1) send NACT (inactive); (2) send INTAK (latch address); (3) put address on bus; (4) send NACT (inactive).





RESET TIMING



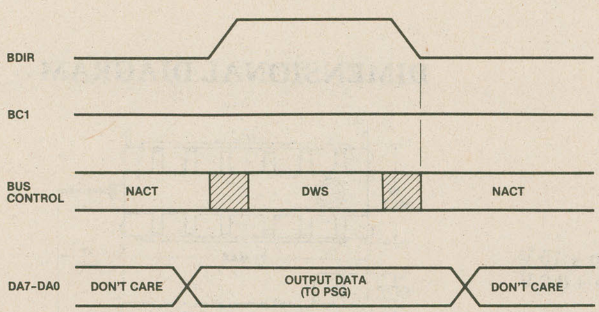
LATCH ADDRESS TIMING

WRITE DATA TO PSG SEQUENCE #1

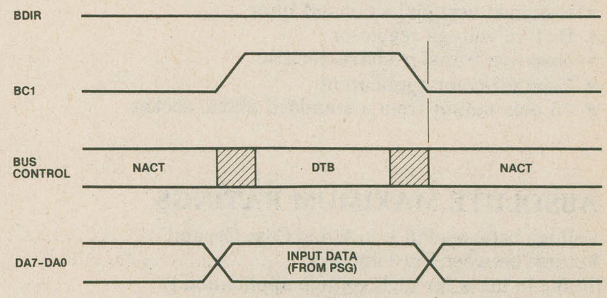
The Write to PSG sequence, which would normally follow immediately after an address sequence, requires four principal microstates: (1) send NACT inactive); (2) put data on bus; (3) send DWS (write to PSG); (4) send NACT (inactive).

READ DATA FROM PSG SEQUENCE #2

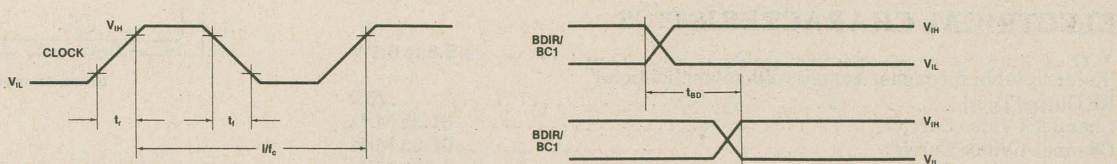
As with the Write to PSG sequence, the Read from PSG sequence would also normally follow immediately after an address sequence. The four principal microstates of the read sequence are: (1) send NACT (inactive); (2) send DTB (read from PSG); (3) read data on bus; (4) send NACT (inactive).



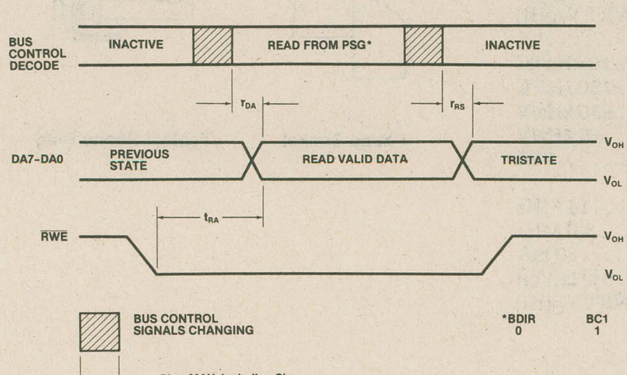
PSG SEQUENCE #1



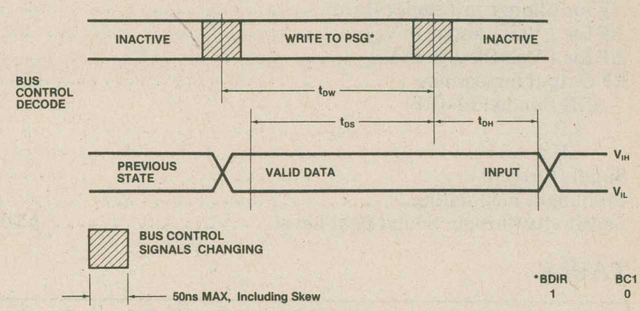
PSG SEQUENCE #2



CLOCK AND BUS SIGNAL TIMING



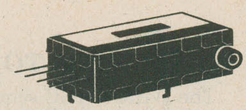
READ DATA TIMING



WRITE DATA TIMING

UM1285-8 VHF MODULATOR

277-221



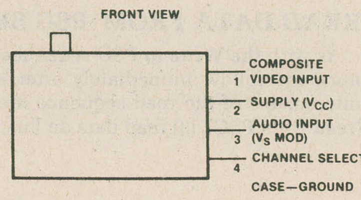
GENERAL DESCRIPTION

The UM1285-8 is a high performance intercarrier vestigial sideband modulator which is primarily intended for use in color TV games, home computer, graphics, teletext and view data adapters. The modulator has a very linear transfer characteristic which ensures good chroma levels and freedom from sync compression and associated frame and line jitter problems, good subcarrier inter modulation performance minimizes the on screen bar pattern due to chroma and sound subcarrier beats.

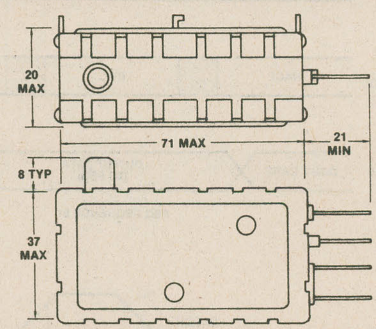
FEATURES

- Compact & low profile
- Rugged & stable
- Good modulation linearity
- Low chroma/sound beat product (55 dB typ)
- Pretuned vision carriers Ch 3, Ch 4
- Pretuned sound subcarrier 4.5 MHz
- Pretuned vestigial sideband filter
- Built-in voltage regulator
- Negative transfer characteristic
- Used for color application
- 75 ohm output from a standard phono socket

PIN CONNECTION



DIMENSIONAL DIAGRAM



Dimensions in mm

ABSOLUTE MAXIMUM RATINGS

Voltage between Pin 1, 3, 4, and Case Ground .... – 3.0 to + 15 V
Voltage between Pin 3 and V_{CC} .... – 3.0 to + 8.0 V
(Refer to table for high voltage application.)
Operating Temperature Range .... 0 to + 45°C
Storage Temperature Range .... – 20 to + 70°C

ELECTRICAL CHARACTERISTICS

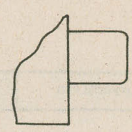
V_{CC} .... + 5.8 to 6.2 V
(Refer to table for higher supply voltage application.)
RF Output Load 75Ω
Channel 3 Video Carrier .... 61.25 MHz
Channel 4 Video Carrier .... 67.65 MHz
Sound Carrier .... 4.500 MHz
Video Carrier output (Vmod = 2.2 V) .... 1.5 mVrms
Video Carrier output (Vmod = 2.8 V) .... 18 dB WRT V_O(HI)
Sound Carrier output .... 22 dB WRT V_O(HI)
Spurious/Harmonic .... 30 dB WRT V_O(HI)
Voltage Standing Wave Ratio (CH 3 and CH 4) 1.7
ΔF for Change in Temperature .... ±10 kHz/°C
ΔF for Change in Temperature .... ±750 Hz/°C
ΔF for 1 Volt Change in V_{CC} .... ±30 kHz/V
ΔF for 1 Volt Change in V_{CC} .... ±5 kHz/V
RF Output Impedance 75Ω
– 3DB Bandwidth (RF)
CH 3 .... 14 MHz
CH 4 .... 5.0 MHz
Supply Current .... 30 mA
Frequency modulating .... 8 kHz/Volt
Sensitivity Chroma/Sound Beat Level .... 55 dB WRT V_O(HI)

TABLE

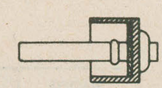
Supply Voltage V_{CC}	Volt	6.0	7.5	9.0	12.0	15.0
Series Resistor R_S	Ohm	0	47	100	180	270

Series resistor with respect to supply voltage

RF OUTPUT SOCKET



Phono Socket



Typical Phono Plug

UM1285-5 277-221

TYPICAL CHARACTERISTICS

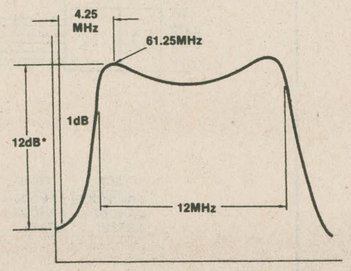
The UM1285-8 is designed to work over a wide range of supply voltage from 6 to 15 V (V_{CC}). A built-in 5.0 V (V_{DD}) voltage regulator is provided to achieve excellent stability against voltage change. A series resistor is recommended between the power source and modulator supply input for the purpose of current limiting.

Modulation occurs when a positive going voltage is applied to the modulation input (video) pin. The transfer characteristic is negative, that means a positive input causes the RF output to decrease. Peak RF output is specified when the video input is at 2.2 V.

RF channel frequency of Ch 3 or Ch 4 can be selected by connecting channel select pin to ground level (0V) to have Ch 3, or open connection to have Ch 4.

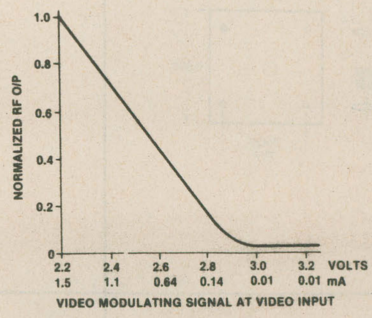
FCC APPROVABLE

The UM1285-8 is FCC approvable due to its very low radiation, stabilized carrier oscillators and vestigial side bank filter which ensures all side band components outside FCC limits are greater than 30 dB down.



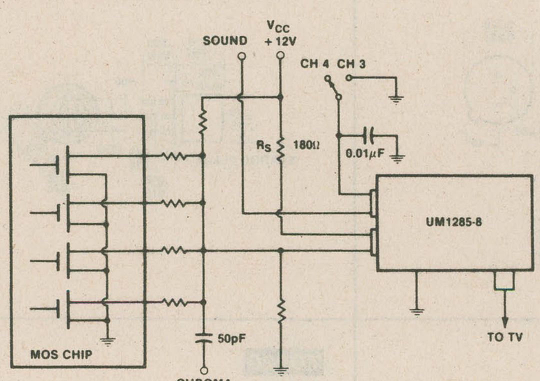
*Note: Subcarriers are > 18dB down wrt carrier at input to bandpass filter giving maximum out of band level of < −30dB wrt carrier.

Typical Bandpass Filter Response

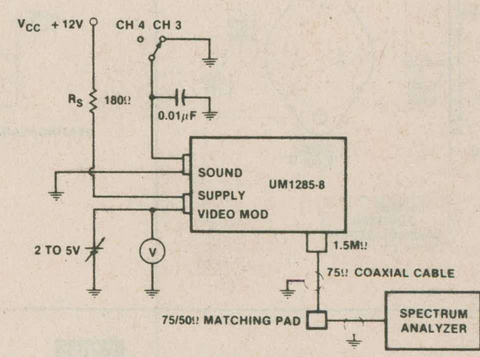


Typical Transfer Characteristic

TYPICAL APPLICATIONS



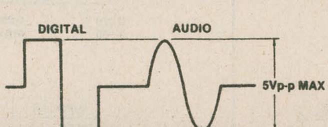
Typical Application



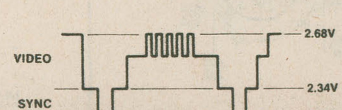
Note: 1. In case of testing with 50Ω I/P spectrum analyzer, matching pad 75/50Ω (attenuation 10dB) should be employed.
2. Standard RF coaxial cable should be 1.5 meters long and 75Ω characteristic impedance.

Test Circuit

TYPICAL INPUT WAVEFORMS



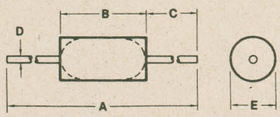
Sound I/P Setup



Modulated Input Voltage Setup

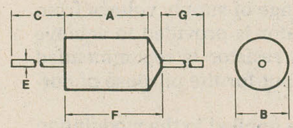
QUICK CASE REFERENCE

A1

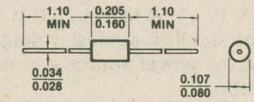


May show color bands to denote polarity.

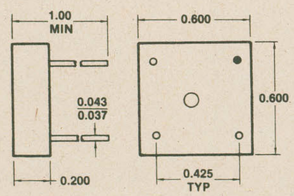
A3



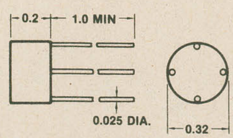
DO41



M532A

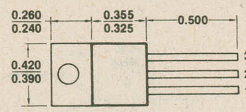


M548



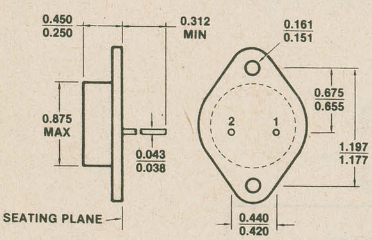
Positive: Red or Square Lead

MU27



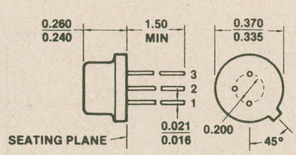
SCR	TRIAC
1-CATHODE	1-ANODE 1
2-ANODE	2-ANODE 2
3-GATE	3-GATE

TO3



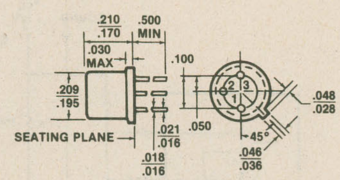
1-BASE
2-EMITTER
CASE-COLLECTOR

TO5

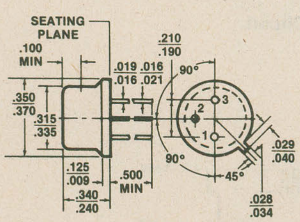


1-EMITTER
2-BASE
3-COLLECTOR

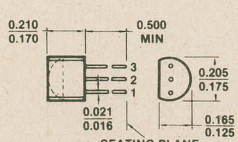
TO18



TO39

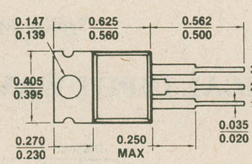


TO92



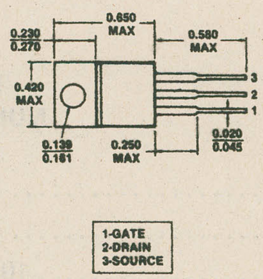
N-CHANNEL FET	UNIJUNCTION	BIPOLAR
1-SOURCE	1-BASE 1	1-EMITTER
2-GATE	2-EMITTER	2-BASE
3-DRAIN	3-BASE 2	3-COLLECTOR

TO220

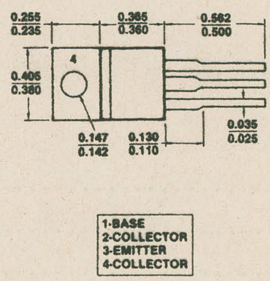


BIPOLAR	TRIAC
1-BASE	1-ANODE 1
2-COLLECTOR	2-ANODE 2
3-EMITTER	3-GATE

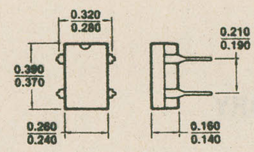
TO220AB



TO220AB-2



Y1



SEMICONDUCTOR CROSS REFERENCE NOTES

N1 Two required, connect in series—anode to anode.
N2 Two required, connect in series—cathode to cathode.
N5 Four required, connect as in original circuit.
N6 Five required, connect as in original circuit.
N7 Six required, connect as in original circuit.

QUICK INDEX

MASTER INDEX BY CATALOG NUMBER

IMPORTANT SUGGESTIONS ON THE USE AND REPLACEMENT OF TRANSISTORS

You can use various styles and sizes of transistors in any given circuit application, as long as the electrical characteristics of the device are within the required range of operation. Thus, a tab-type device can be used to replace a TO-3 or TO-66 case device; or a small epoxy-type device can be used in place of TO-5 or other size transistor.

Generally speaking, you must observe the following maximum characteristics of a transistor when contemplating substitution or selection:

Power dissipation
Maximum collector current
Maximum collector-to-emitter voltage
Maximum collector-to-base voltage
Maximum emitter-to-base voltage

Also, it is useful to consider the following characteristics for actual circuit operation:

Gain
Frequency limitations

Caution: It may be necessary in some cases to adjust bias values to achieve required operation. With tuned circuits, it is a good practice to check alignment after replacing any transistor.

When replacing power transistors, always check driver devices to be sure they are OK. Also, check other circuit components to be sure they were not shorted (or otherwise defective) when the original device failed. If you fail to correct such problems before applying power to the circuit once again, the replacement transistor could easily be permanently damaged. Be sure to use proper heat-sink precautions and use silicon grease to reduce the thermal resistance between the case of the transistor and the heat-sink.

Always observe temperature limitations as specified with transistor ratings.

It almost goes without saying, but let us remind you anyway—

Always observe voltage polarity with all semiconductor devices.

CROSS-REFERENCE/SUBSTITUTION LISTING

Most users of semiconductors realize that it is almost impossible to guarantee absolute equivalents (as in the case of tubes). Thus, the only way to create replacement or cross-reference listings is by carefully evaluating each characteristic of both devices (original transistor and the possible alternate). This is how the Technical Staff of Radio Shack went about preparing the following cross-reference/replacement lists.

IMPORTANT NOTE

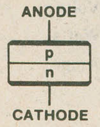
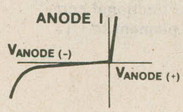
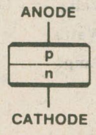
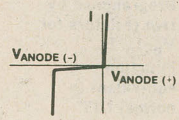
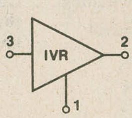
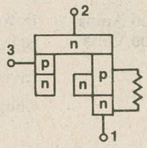
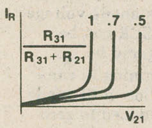
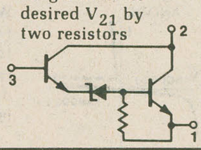
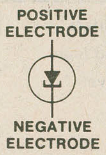
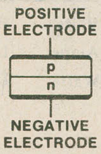
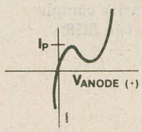
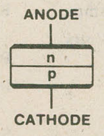
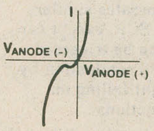
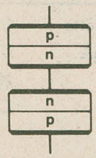
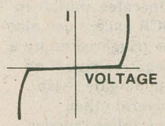
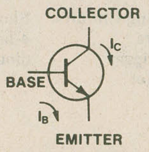
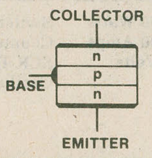
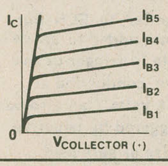
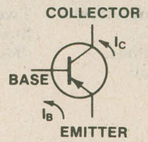
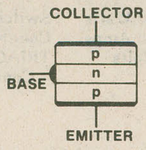
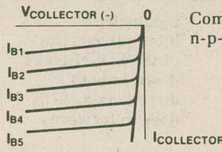
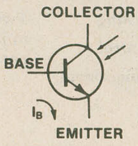
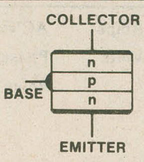
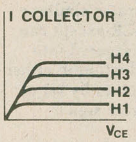
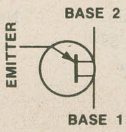
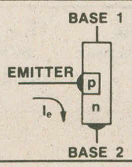
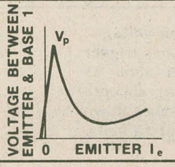
We caution you that in many cases the listed cross reference ARCHER device may be different in appearance, size or mounting style. Thus, before beginning replacement or installation procedures, check to be sure you have enough room for proper mounting.

Also, when making substitutions or replacements in radio or high frequency circuitry, it may be necessary to realign tunable circuit elements. This is true even when making **exact** replacements (junction capacitances normally vary between devices even from the same production run).

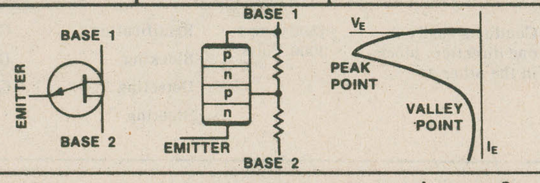
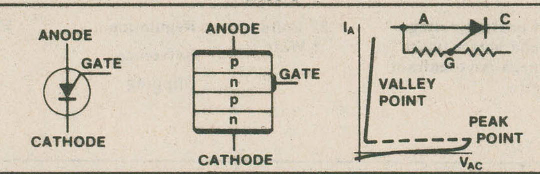
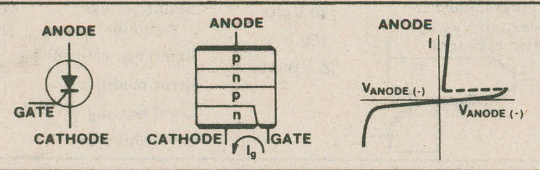
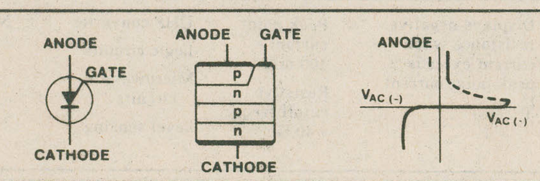
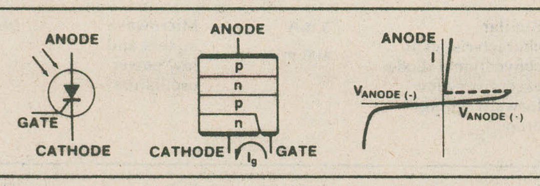
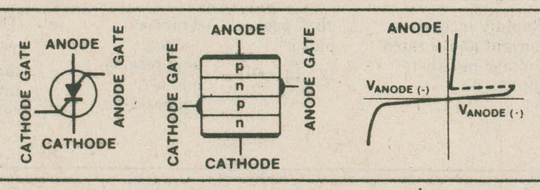
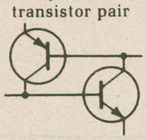
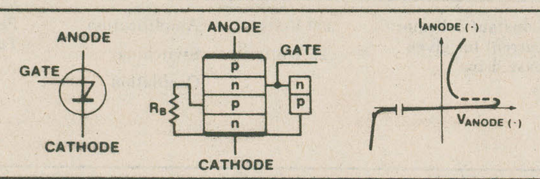
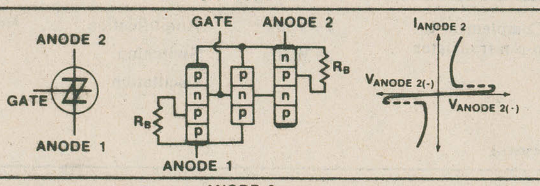
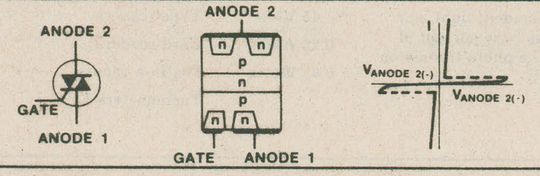
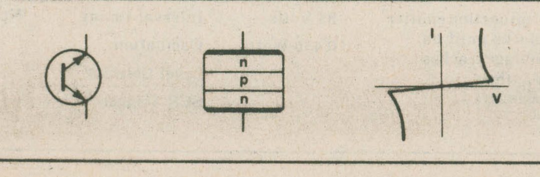
Information contained in this guide is based on the latest available data and is believed to be accurate. Every care has been taken to assure technical accuracy. However, Radio Shack does not assume responsibility for any contingencies of the use of this information. Nor does Radio Shack assume any responsibility for any infringements of patents or other rights of third parties which may result from its use.

When you are looking for a specific number and it does not show up in the following listing—refer to the technical data provided for our line of ARCHER devices. With this information you probably will be able to make a suitable substitution.

MAJOR SEMICONDUCTOR COMPONENTS

NAME OF DEVICE	CIRCUIT SYMBOL	COMMONLY USED JUNCTION SCHEMATIC	ELECTRICAL CHARACTERISTICS		MAX RATINGS AVAILABLE	MAJOR APPLICATIONS	ROUGHLY ANALOGOUS TO:
Diode or Rectifier				Conducts easily in one direction, blocks in the other	1500 Amps 3000 Volts	Rectification Blocking Detecting Steering	Check valve Diode tube Gas diode
Avalanche (Zener) Diode				Constant voltage characteristic in negative quadrant	22 Volts 1 Watt	Regulation Reference Clipping	V-R tube
Integrated Voltage Regulator (IVR)				Programmed to desired V_{21} by two resistors 	40 Volts 100 mA 0.4 Watts	Shunt voltage regulator Reference element Error modifier Level sensing Level shifting	Avalanche Diode
Tunnel Diode				Displays negative resistance when current exceeds peak point current I_p	Peak point current = 100 mA Resistive cutoff freq. = 40 Gc	UHF converter Logic circuits Microwave circuits Level sensing	None
Back Diode				Similar characteristics to conventional diode except very low forward voltage drop	5 mA 400 mV	Microwave mixers and low power oscillators	None
Thyrector				Rapidly increasing current above rated voltage in either direction	70 A peak pulse (2" Sq. cell)	Transient voltage suppression and arc suppression	Thyrite Two avalanche diodes in inverse-series connection
n-p-n Transistor				Constant collector current for given base drive	300 Volts 25 Watts	Amplification Switching Oscillation	Pentode Tube
p-n-p Transistor				Complement to n-p-n transistor	75 Volts 25 Watts	Amplification Switching Oscillation	None
Photo Transistor				Incident light acts as base current of the photo transistor	45 Volts 0.25 Amps 0.6 Watts	Tape readers Card readers Position sensor Tachometers	None
Unijunction Transistor (UJT)				Unijunction emitter blocks until its voltage reaches V_p; then conducts	35 Volts 0.450 Watts	Interval timing Oscillation Level Detector SCR Trigger	None

MAJOR SEMICONDUCTOR COMPONENTS

NAME OF DEVICE	CIRCUIT SYMBOL	COMMONLY USED JUNCTION SCHEMATIC	ELECTRICAL CHARACTERISTICS	MAX RATINGS AVAILABLE	MAJOR APPLICATIONS	ROUGHLY ANALOGOUS TO:
Complementary Unijunction Transistor (CUJT)			Functional complement to UJT	30 Volts 0.30 Watts 0.15 Amps	High stability timers Oscillators and level detectors	None
Programmable Unijunction Transistor (PUT)			Programmed by two resistors for V_p, I_p, I_v. Function equivalent to normal UJT.	40 Volts 0.30 Watts 0.15 Amps	Low cost timers and oscillators Long period timers SCR trigger Level detector	UJT
Silicon Controlled Rectifier (SCR)			With anode voltage (+), SCR can be triggered by I_g, remaining in conduction until anode I is reduced to zero	1000 Amps 1800 Volts	Power switching Phase control Inverters Choppers	Gas thyratron or ignitron
Complementary Silicon Controlled Rectifier (CSCR)			Polarity complement to SCR	50 Volts 0.25 Amps 0.45 Watts	Ring counters Low speed logic Lamp driver	None
Light Activated SCR* (LASCR)			Operates similar to SCR, except can also be triggered into conduction by light falling on junctions	1.6 Amps 200 Volts	Relay Replacement Position controls Photoelectric applications Slave flashes	None
Silicon Controlled Switch* (SCS)			Operates similar to SCR except can also be triggered on by a negative signal on anode-gate. Also several other specialized modes of operation	100 Volts 200 mA	Logic applications Counters Nixie drivers Lamp drivers	Complementary transistor pair 
Silicon Unilateral Switch (SUS)			Similar to SCS but zener added to anode gate to trigger device into conduction at ~ 8 volts. Can also be triggered by negative pulse at gate lead.	0.350 Watts 0.200 Amps 10 Volts	Switching Circuits Counters SCR Trigger Oscillator	Shockley or 4-layer diode
Silicon Bilateral Switch (SBS)			Symmetrical bilateral version of the SUS. Breaks down in both directions as SUS does in forward.	0.350 Watts 0.200 Amps 10 Volts	Switching Circuits Counters TRIAC Phase Control	Two inverse Schockley diodes
Triac			Operates similar to SCR except can be triggered into conduction in either direction by (+) or (-) gate signal	25 Amps 500 Volts	AC switching Phase control Relay replacement	Two SCR's in inverse parallel
Diac Trigger			When voltage reaches trigger level (about 35 volts), abruptly switches down about 10 volts.	40 Volts 2 Amps peak	Triac and SCR trigger Oscillator	Neon lamp

*Light Activated SCS also available.

GLOSSARY OF WORDS, SYMBOLS AND ABBREVIATIONS

The following letter symbols and abbreviations are recommended by the Joint Electron Device Engineering Council (JEDEC) of the Electronic Industries Association (EIA) and the National Electrical Manufacturers Association (NEMA) for use in semiconductor device data sheets and specifications.

A, a —Anode
B, b —Base
b_{fs} —Common-source small-signal forward transfer susceptance
b_{is} —Common-source small-signal input susceptance
b_{os} —Common-source small-signal output susceptance
b_{rs} —Common-source small-signal reverse transfer susceptance
C, c —Collector
C_{cb} —Collector-base interterminal capacitance
C_{ce} —Collector-emitter interterminal capacitance
C_{ds} —Drain-source capacitance
C_{du} —Drain-substrate capacitance
C_{eb} —Emitter-base interterminal capacitance
C_{ibo} —Common-base open-circuit input capacitance
C_{ibs} —Common-base short-circuit input capacitance
C_{ieo} —Common-emitter open-circuit input capacitance
C_{ies} —Common-emitter short-circuit input capacitance
C_{iss} —Common-source short-circuit input capacitance
C_{obo} —Common-base open-circuit output capacitance
C_{obs} —Common-base short-circuit output capacitance
C_{oeo} —Common-emitter open-circuit output capacitance
C_{oes} —Common-emitter short-circuit output capacitance
C_{oss} —Common-source short-circuit output capacitance
C_{rbs} —Common-base short-circuit reverse transfer capacitance
C_{rcs} —Common-collector short-circuit reverse transfer capacitance
C_{res} —Common-emitter short-circuit reverse transfer capacitance
C_{rss} —Common-source short-circuit reverse transfer capacitance
C_{tc} —Collector depletion-layer capacitance
C_{te} —Emitter depletion-layer capacitance
D, d —Drain
E, e —Emitter
η —Intrinsic standoff ratio
f_{hfb} —Common-base small-signal short-circuit forward current transfer ratio cutoff frequency
f_{hfc} —Common-collector small-signal short-circuit forward current transfer ratio cutoff frequency
f_{hfe} —Common-emitter small-signal short-circuit forward current transfer ratio cutoff frequency
f_{max} —Maximum frequency of oscillation
F_T —Transition frequency (frequency at which common-emitter small-signal forward current transfer ratio extrapolates to unity)
G, g —Gate
g_{fs} —Common-source small-signal forward transfer conductance
g_{is} —Common-source small-signal input conductance
g_{MB} —Common-base static transconductance
g_{MC} —Common-collector static transconductance
g_{ME} —Common-emitter static transconductance
g_{os} —Common-source small-signal output conductance
G_{PB} —Common-base large-signal insertion power gain
G_{pb} —Common-base small-signal insertion power gain
G_{PC} —Common-collector large-signal insertion power gain
G_{pc} —Common-collector small-signal insertion power gain
G_{PE} —Common-emitter large-signal insertion power gain
G_{pe} —Common-emitter small-signal insertion power gain
G_{pg} —Common-gate small-signal insertion power gain
G_{ps} —Common-source small-signal insertion power gain
g_{rs} —Common-source small-signal reverse transfer conductance
G_{TB} —Common-base large-signal transducer power gain
G_{tb} —Common-base small-signal transducer power gain
G_{TC} —Common-collector large-signal transducer power gain
G_{tc} —Common-collector small-signal transducer power gain
G_{TE} —Common-emitter large-signal transducer power gain
G_{te} —Common-emitter small-signal transducer power gain
G_{tg} —Common-gate small-signal transducer power gain
G_{ts} —Common-source small-signal transducer power gain
h_{FB} —Common-base static forward current transfer ratio
h_{fb} —Common-base small-signal short-circuit forward current transfer ratio
h_{FC} —Common-collector static forward current transfer ratio
h_{fc} —Common-collector small-signal short-circuit forward current transfer ratio
h_{FE} —Common-emitter static forward current transfer ratio
h_{fe} —Common-emitter small-signal short-circuit forward current transfer ratio
h_{FEL} —Inherent large-signal forward current transfer ratio
h_{IB} —Common-base static input resistance
h_{ib} —Common-base small-signal short-circuit input impedance
h_{IC} —Common-collector static input resistance
h_{ic} —Common-collector small-signal short-circuit input impedance
h_{IE} —Common-emitter static input resistance
h_{ie} —Common-emitter small-signal short-circuit input impedance
$h_{ie(imag)}$ —Imaginary part of common-emitter small-signal short-circuit input impedance
$h_{ie(real)}$ —Real part of common-emitter small-signal short-circuit input impedance
h_{ob} —Common-base small-signal open-circuit output admittance
h_{oc} —Common-collector small-signal open-circuit output admittance
h_{oe} —Common-emitter small-signal open-circuit output admittance
$h_{oe(imag)}$ —Imaginary part of common-emitter small-signal open-circuit output admittance

$h_{oe(real)}$ —Real part of common-emitter small-signal open-circuit output admittance

h_{rb} —Common-base small-signal open-circuit reverse voltage transfer ratio

h_{rc} —Common-collector small-signal open-circuit reverse voltage transfer ratio

h_{re} —Common-emitter small-signal open-circuit reverse voltage transfer ratio

I_B —Base-terminal dc current

I_b —Alternating component (rms value) of base-terminal current

i_B —Instantaneous total value of base-terminal current

I_{BEV} —Base cutoff current, dc

$I_{B2(mod)}$ —Interbase modulated current

I_C —Collector-terminal dc current

I_c —Alternating component (rms value) of collector-terminal current

i_C —Instantaneous total value of collector-terminal current

I_{CBO} —Collector cutoff current (dc), emitter open

I_{CEO} —Collector cutoff current (dc), base open

I_{CER} —Collector cutoff current (dc), specified resistance between base and emitter

I_{CES} —Collector cutoff current (dc), base shorted to emitter

I_{CEV} —Collector cutoff current (dc), specified voltage between base and emitter

I_{CEX} —Collector cutoff current (dc), specified circuit between base and emitter

I_D —Drain current, dc

$I_{D(off)}$ —Drain cutoff current

$I_{D(on)}$ —On-state drain current

I_{DSS} —Zero-gate-voltage drain current

I_E —Emitter-terminal dc current

I_e —Alternating component (rms value) of emitter-terminal current

i_E —Instantaneous total value of emitter-terminal current

I_{EBO} —Emitter cutoff current (dc), collector open

I_{EB2O} —Emitter reverse current

$I_{EC(ofs)}$ —Emitter-collector offset current

I_{ECS} —Emitter cutoff current (dc), base short-circuited to collector

$I_{E1E2(off)}$ —Emitter cutoff current

I_F —For voltage-regulator and voltage-reference diodes: dc forward current. For signal diodes and rectifier diodes: dc forward current (no alternating component)

I_f —Alternating component of forward current (rms value)

i_F —Instantaneous total forward current

$I_{F(AV)}$ —Forward current, dc (with alternating component)

I_{FM} —Maximum (peak) total forward current

$I_{F(OV)}$ —Forward current, overload

I_{FRM} —Maximum (peak) forward current, repetitive

$I_{F(RMS)}$ —Total rms forward current

I_{FSM} —Maximum (peak) forward current, surge

I_G —Gate current, dc

I_{GF} —Forward gate current

I_{GR} —Reverse gate current

I_{GSS} —Reverse gate current, drain short-circuited to source

I_{GSSF} —Forward gate current, drain short-circuited to source

I_{GSSR} —Reverse gate current, drain short-circuited to source

I_I —Inflection-point current

$Im(h_{ie})$ —Imaginary part of common-emitter small-signal short-circuit input impedance

$Im(h_{oe})$ —Imaginary part of common-emitter small-signal open-circuit output admittance

I_O —Average forward current, 180° conduction angle, 60-Hz half sine wave

I_P —Peak-point current

I_R —For voltage-regulator and voltage-reference diodes: dc reverse current. For signal diodes and rectifier diodes: dc reverse current (no alternating component)

I_r —Alternating component of reverse current (rms value)

i_R —Instantaneous total reverse current

$I_{R(AV)}$ —Reverse current, dc (with alternating component)

I_{RM} —Maximum (peak) total reverse current

I_{RRM} —Maximum (peak) reverse current, repetitive

$I_{R(RMS)}$ —Total rms reverse current

I_{RSM} —Maximum (peak) surge reverse current

I_S —Source current, dc

I_{SDS} —Zero-gate-voltage source current

$I_{S(off)}$ —Source cutoff current

I_V —Valley-point current

I_Z —Regulator current, reference current (dc)

I_{ZK} —Regulator current, reference current (dc near breakdown knee)

I_{ZM} —Regulator current, reference current (dc maximum rated current)

K, k —Cathode

L_c —Conversion loss

M —Figure of merit

NF_o —Overall noise figure

NR_o —Output noise ratio

P_{BE} —Power input (dc) to base, common emitter

p_{BE} —Instantaneous total power input to base, common emitter

P_{CB} —Power input (dc) to collector, common base

p_{CB} —Instantaneous total power input to collector, common base

P_{CE} —Power input (dc) to collector, common emitter

p_{CE} —Instantaneous total power input to collector, common emitter

P_{EB} —Power input (dc) to emitter, common base

p_{EB} —Instantaneous total power input to emitter, common base

P_F —Forward power dissipation, dc (no alternating component)

p_F —Instantaneous total forward power dissipation

$P_{F(AV)}$ —Forward power dissipation, dc (with alternating component)

P_{FM} —Maximum (peak) total forward power dissipation

P_{IB} —Common-base large-signal input power

p_{ib} —Common-base small-signal input power

P_{IC} —Common-collector large-signal input power

p_{ic} —Common-collector small-signal input power

P_{IE} —Common-emitter large-signal input power

p_{ie} —Common-emitter small-signal input power

P_{OB} —Common-base large-signal output power

p_{ob} —Common-base small-signal output power

P_{OC} —Common-collector large-signal output power

p_{oc} —Common-collector small-signal output power

P_{OE} —Common-emitter large-signal output power

p_{oe} —Common-emitter small-signal output power

P_R —Reverse power dissipation, dc (no alternating component)

p_R —Instantaneous total reverse power dissipation

$P_{R(AV)}$ —Reverse power dissipation, dc (with alternating component)

P_{RM} —Maximum (peak) total reverse power dissipation

P_T —Total nonreactive power input to all terminals

p_T —Nonreactive power input, instantaneous total, to all terminals

Q_S —Stored charge

r_{BB} —Interbase resistance

r_bC_c —Collector-base time constant

$r_{CE(sat)}$ —Saturation resistance, collector-to-emitter

$r_{DS(on)}$ —Static drain-source on-state resistance

$r_{ds(on)}$ —Small-signal drain-source on-state resistance

$Re(h_{ie})$ —Real part of common-emitter small-signal short-circuit input impedance

$Re(h_{oe})$ —Real part of common-emitter small-signal open-circuit output admittance

$r_{e1e2(on)}$ —Small-signal emitter-emitter on-state resistance

r_i —Dynamic resistance at inflection point

R_θ —Thermal resistance

$R_{\theta CA}$ —Thermal resistance, case to ambient

$R_{\theta JA}$ —Thermal resistance, junction to ambient

$R_{\theta JC}$ —Thermal resistance, junction to case

S, s —Source

T_A —Ambient temperature or free-air temperature

T_C —Case temperature

t_d —Delay time

$t_{d(off)}$ —Turn-off delay time

$t_{d(on)}$ —Turn-on delay time

t_f —Fall time

t_{fr} —Forward recovery time

T_j —Junction temperature

t_{off} —Turn-off time

t_{on} —Turn-on time

t_p —Pulse time

t_r —Rise time

t_{rr} —Reverse recovery time

t_s —Storage time

TSS —Tangential signal sensitivity

T_{stg} —Storage temperature

t_w —Pulse average time

U, u —Bulk (substrate)

V_{BB} —Base supply voltage (dc)

V_{BC} —Average or dc voltage, base to collector

V_{bc} —Instantaneous value of alternating component of base-collector voltage

V_{BE} —Average or dc voltage, base to emitter

v_{be} —Instantaneous value of alternating component of base-emitter voltage

$V_{(BR)}$ —Breakdown voltage (dc)

$v_{(BR)}$ —Breakdown voltage (instantaneous total)

$V_{(BR)CBO}$ —Collector-base breakdown voltage, emitter open

$V_{(BR)CEO}$ —Collector-emitter breakdown voltage, base open

$V_{(BR)CER}$ —Collector-emitter breakown voltage, resistance between base and emitter

$V_{(BR)CES}$ —Collector-emitter breakdown voltage, base shorted to emitter

$V_{(BR)CEV}$ —Collector-emitter breakdown voltage, specified voltage between base and emitter

$V_{(BR)CEX}$ —Collector-emitter breakdown voltage, specified circuit between base and emitter

$V_{(BR)EBO}$ —Emitter-base breakdown voltage, collector open

$V_{(BR)ECO}$ —Emitter-collector breakdown voltage, base

$V_{(BR)E1E2}$ —Emitter-emitter breakdown voltage

$V_{(BR)GSS}$ —Gate-source breakdown voltage

$V_{(BR)GSSF}$ —Forward gate-source breakdown voltage

$V_{(BR)GSSR}$ —Reverse gate-source breakdown voltage

V_{B2B1} —Interbase voltage

V_{CB} —Average or dc voltage, collector to base

v_{cb} —Instantaneous value of alternating component of collector-base voltage

$V_{CB(fl)}$ —Collector-base dc open-circuit voltage (floating potential)

V_{CBO} —Collector-base voltage, dc, emitter open

V_{CC} —Collector supply voltage (dc)

V_{CE} —Average or dc voltage, collector to emitter

v_{ce} —Instantaneous value of alternating component of collector-emitter voltage

$V_{CE(fl)}$ —Collector-emitter dc open-circuit voltage (floating potential)

V_{CEO} —Collector-emitter voltage (dc), base open

$V_{CE(ofs)}$ —Collector-emitter offset voltage

V_{CER} —Collector-emitter voltage (dc), resistance between base and emitter

V_{CES} —Collector-emitter voltage (dc), base shorted to emitter

$V_{CE(sat)}$ —Collector-emitter dc saturation voltage

V_{CEV} —Collector-emitter voltage (dc), specified voltage between base and emitter

V_{CEX} —Collector-emitter voltage (dc), specified circuit between base and emitter

V_{DD} —Drain supply voltage (dc)

V_{DG} —Drain-gate voltage

V_{DS} —Drain-source voltage

$V_{DS(on)}$ —Drain-source on-state voltage

V_{DU} —Drain-substrate voltage

V_{EB} —Average or dc voltage, emitter to base

v_{eb} —Instantaneous value of alternating component of emitter-base voltage

$V_{EB(fl)}$ —Emitter-base dc open-circuit voltage (floating potential)

V_{EBO} —Emitter-base voltage (dc), collector open

$V_{EB1(sat)}$ —Emitter saturation voltage

V_{EC} —Average or dc voltage, emitter to collector

v_{ec} —Instantaneous value of alternating component of emitter-collector voltage

$V_{EC(fl)}$ —Emitter-collector dc open-circuit voltage (floating potential)

$V_{EC(ofs)}$ —Emitter-collector offset voltage

V_{EE} —Emitter supply voltage (dc)

V_F —For voltage-regulator and voltage-reference diodes: dc forward voltage. For signal diodes and rectifier diodes: dc forward voltage (no alternating component)

V_f —Alternating component of forward voltage (rms value)

v_F —Instantaneous total forward voltage

$V_{F(AV)}$ —Forward voltage, dc (with alternating component)

V_{FM} —Maximum (peak) total forward voltage

$V_{F(RMS)}$ —Total rms forward voltage

V_{GG} —Gate supply voltage (dc)

V_{GS} —Gate-source voltage

V_{GSF} —Forward gate-source voltage

$V_{GS(off)}$ —Gate-source cutoff voltage

V_{GSR} —Reverse gate-source voltage

$V_{GS(th)}$ —Gate-source threshold voltage

V_{GU} —Gate-substrate voltage

V_I —Inflection-point voltage

V_{OB1} —Base-1 peak voltage

V_P —Peak-point voltage

V_{PP} —Projected peak-point voltage

V_R —For voltage-regulator and voltage-reference diodes: dc reverse voltage. For signal diodes and rectifier diodes: dc reverse voltage (no alternating component)

V_r —Alternating component of reverse voltage (rms value)

v_R —Instantaneous total reverse voltage
$V_{R(AV)}$ —Reverse voltage, dc (with alternating component)
V_{RM} —Maximum (peak) total reverse voltage
V_{RRM} —Repetitive peak reverse voltage
$V_{R(RMS)}$ —Total rms reverse voltage
V_{RSM} —Nonrepetitive peak reverse voltage
V_{RT} —Reach-through voltage
V_{RWM} —Working peak reverse voltage
V_{SS} —Source supply voltage (dc)
V_{SU} —Source-substrate voltage
$V_{(TO)}$ —Threshold voltage
V_V —Valley-point voltage
V_Z —Regulator voltage, reference voltage (dc)
V_{ZM} —Regulator voltage, reference voltage (dc at maximum rated current)
y_{fb} —Common-base small-signal short-circuit forward transfer admittance
y_{fc} —Common-collector small-signal short-circuit forward transfer admittance
y_{fe} —Common-emitter small-signal short-circuit forward transfer admittance
y_{fs} —Common-source small-signal short-circuit forward transfer admittance
$y_{fs(imag)}$ —Common-source small-signal forward transfer susceptance
$y_{fs(real)}$ —Common-source small-signal forward transfer conductance
y_{ib} —Common-base small-signal short-circuit input admittance
y_{ic} —Common-collector small-signal short-circuit input admittance
y_{ie} —Common-emitter small-signal short-circuit input admittance
$y_{ie(imag)}$ —Imaginary part of small-signal short-circuit input admittance (common-emitter)
$y_{ie(real)}$ —Real part of small-signal short-circuit input admittance (common-emitter)
y_{is} —Common-source small-signal short-circuit input admittance
$y_{is(imag)}$ —Common-source small-signal input susceptance
$y_{is(real)}$ —Common-source small-signal input conductance
y_{ob} —Common-base small-signal short-circuit output admittance
y_{oc} —Common-collector small-signal short-circuit output admittance
y_{oe} —Common-emitter small-signal short-circuit output admittance
$y_{oe(imag)}$ —Imaginary part of small-signal short-circuit output admittance (common-emitter)
$y_{oe(real)}$ —Real part of small-signal short-circuit output admittance (common-emitter)
y_{os} —Common-source small-signal short-circuit output admittance
$y_{os(imag)}$ —Common-source small-signal output susceptance
$y_{os(real)}$ —Common-source small-signal output conductance
y_{rb} —Common-base small-signal short-circuit reverse transfer admittance
y_{rc} —Common-collector small-signal short-circuit reverse transfer admittance
y_{re} —Common-emitter small-signal short-circuit reverse transfer admittance
y_{rs} —Common-source small-signal short-circuit reverse transfer admittance
$y_{rs(imag)}$ —Common-source small-signal reverse transfer susceptance
$y_{rs(real)}$ —Common-source small-signal reverse transfer conductance
z_{if} —Intermediate-frequency impedance
z_m —Modulator-frequency load impedance
z_{rf} —Radio-frequency impedance
$Z_{\theta JA(t)}$ —Junction-to-ambient transient thermal impedance
$Z_{\theta JC(t)}$ —Junction-to-case transient thermal impedance
$Z_{\theta(t)}$ —Transient thermal impedance
z_v —Video impedance
z_z —Regulator impedance, reference impedance (small-signal at I_z)
z_{zk} —Regulator impedance, reference impedance (small-signal at I_{ZK})
z_{zm} —Regulator impedance, reference impedance (small-signal at I_{ZM})

PREFIX AND MANUFACTURER IDENTIFICATION

PREFIX	MANUFACTURER	PREFIX	MANUFACTURER	PREFIX	MANUFACTURER
BA	Rohm	MOC	Motorola	SLP	Sanyo
CEX	Control Electronics	MPS	Motorola	SN	Texas Instruments
DAC	National Semiconductor	MRF	Motorola	TA	Toshiba
FND	Fairchild	MU	Motorola	TIL	Texas Instruments
FRL	Litronix	MV	General Instrument	TIP	Motorola
ICM	Intersil	NE	Signetics	TLO	Texas Instruments
LF	National Semiconductor	NSM	National Semiconductor	TL	Texas Instruments
LM	National Semiconductor	PCIM	PC International	TLG	Toshiba
MA	National Semiconductor	S	American Micro Systems	TLR	Toshiba
MC	Motorola	SAD	Reticon	VN	Siliconix
MJ	Motorola	SE	Signetics	XC	Xciton
MM	National Semiconductor. Motorola or Teledyne	SEL	Sanken		
		SCS	Spectronics		

GENERIC PART NUMBER PREFIX CODE

AD	Analog To Digital	DA	Digital To Analog	LM	Linear Monolithic
AH	Analog Hybrid	DM	Digital Monolithic	MM	MOS Monolithic
AM	Analog Monolithic	LF	Linear FET	TBA	Linear Monolithic
CD	CMOS Digital	LH	Linear Hybrid		